Timed Games for Computing WCET on Pipelined Processors with Caches

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Outline of the talk

1. The Worst-Case Execution-Time Problem
2. Modular Computation of WCET
3. Experiments & Results
4. Conclusion & Future Work

Worst-Case Execution-Time

Input data
$d \in \mathcal{D}$

Program P

```
10: e3a03000    mov   r3, #0
14: e58d3014    str   r3, [sp, #20]
18: e3a03002    mov   r3, #2
1c: e58d300c    str   r3, [sp, #12]
20: ea00000a    b     50 <fib+0x50>
24: e59d3010    ldr   r3, [sp, #16]
28: e58d3018    str   r3, [sp, #24]
2c: e59d2010    ldr   r2, [sp, #16]
30: e59d3014    ldr   r3, [sp, #20]
34: e0823003    add   r3, r2, r3
38: e58d3010    str   r3, [sp, #16]
3c: e59d3018    ldr   r3, [sp, #24]
40: e58d3014    str   r3, [sp, #20]
44: e59d300c    ldr   r3, [sp, #12]
48: e2833001    add   r3, r3, #1
4c: e58d300c    str   r3, [sp, #12]
50: e59d200c    ldr   r2, [sp, #12]
54: e59d3004    ldr   r3, [sp, #4]
58: e1520003    cmp   r2, r3
5c: dafffff0    ble   24 <fib+0x24>
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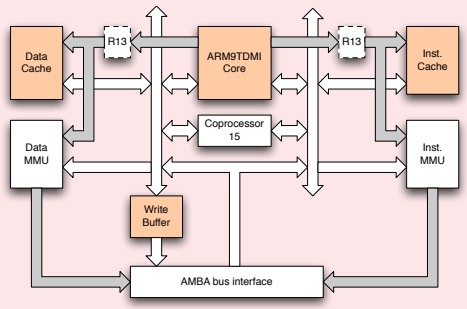
Hardware H



→ time(H, P, d)

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$d \in \mathcal{D}$

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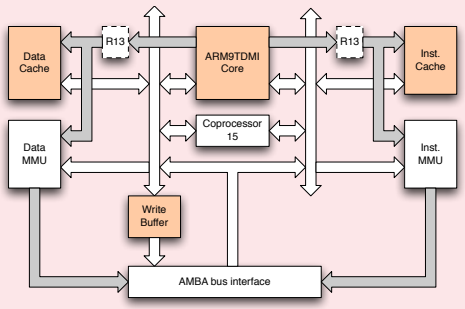

→ time(H, P, d)

$$WCET(H, P) = \max_{d \in \mathcal{D}} time(H, P, d)$$

Worst-Case Execution-Time

Input data
$d \in \mathcal{D}$

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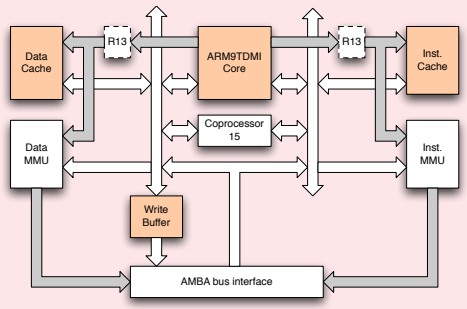

→ time(H, P, d)

$$WCET(H,P) \leq WCET\text{-}UB(H,P) \leq (1+\varepsilon) \times WCET(H,P)$$

Related Work & Existing Methods

Partial – Tests/Simulation

- random
- probabilistic
- real board, simulator

- easy to implement
- not exhaustive
- not safe: gives a lower bound

Tools: RapiTime (based on pWCET) and Mtime

Exhaustive – Static Analysis & Integer Linear Programming

1. Compute a control flow graph of P
2. Determine loop upper bounds
3. Build a weighted CFG
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- harder to implement
- safe: gives an upper bound
- manual annotations
- algorithm is monolithic

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Our Contribution

Assumptions on binary program P:

- termination of P does not depend on input data
- P always terminates

Results

- Fully automatic computation of WCET
  computation of CFG (and stack size)
  computation of WCET-equivalent program
- Modular method
  1. Program model
  2. Hardware model
  3. Analysis (computation of WCET)
- Comparison of computed WCET and actual WCET
  WCET Benchmarks from Mälardalen University
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  WCET computed with UPPAAL

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The Fibonacci Program

```
00000000 <fib>:
   0:  e24dd020     sub   sp, sp, #32
   4:  e58d0004     str   r0, [sp, #4]
   8:  e3a03001     mov   r3, #1
   c:  e58d3010     str   r3, [sp, #16]
  10:  e3a03000     mov   r3, #0
  14:  e58d3014     str   r3, [sp, #20]
  18:  e3a03002     mov   r3, #2
  1c:  e58d300c     str   r3, [sp, #12]
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  24:  e59d3010     ldr   r3, [sp, #16]
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  5c:  dafffff0     ble   24 <fib+0x24>
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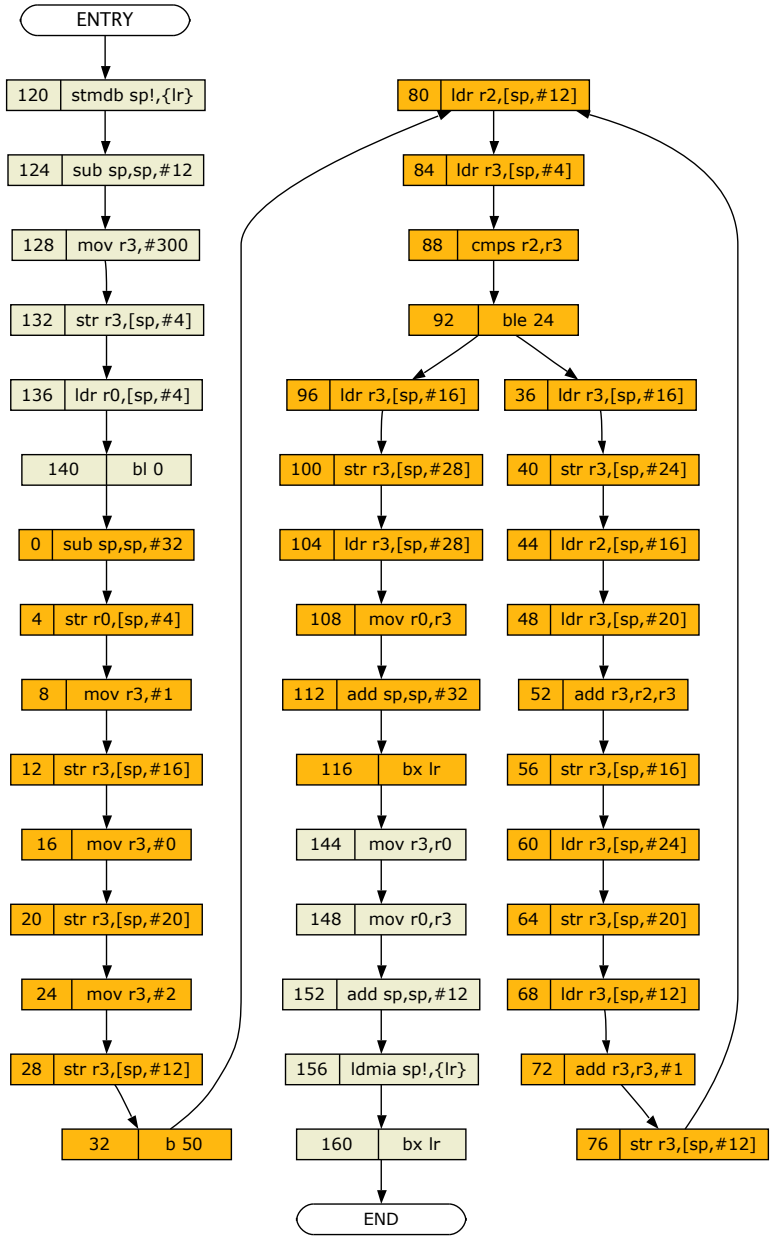
  64:  e58d301c     str   r3, [sp, #28]
  68:  e59d301c     ldr   r3, [sp, #28]
  6c:  e1a00003     mov   r0, r3
  70:  e28dd020     add   sp, sp, #32
  74:  e12fff1e     bx    lr

00000078 <main>:
  78:  e52de004     push  {lr}
  7c:  e24dd00c     sub   sp, sp, #12
  80:  e3a03f4b     mov   r3, #300
  84:  e58d3004     str   r3, [sp, #4]
  88:  e59d0004     ldr   r0, [sp, #4]
  8c:  ebffffdb     bl    0 <fib>
  90:  e1a03000     mov   r3, r0
  94:  e1a00003     mov   r0, r3
  98:  e28dd00c     add   sp, sp, #12
  9c:  e49de004     pop   {lr}
  a0:  e12fff1e     bx    lr
```



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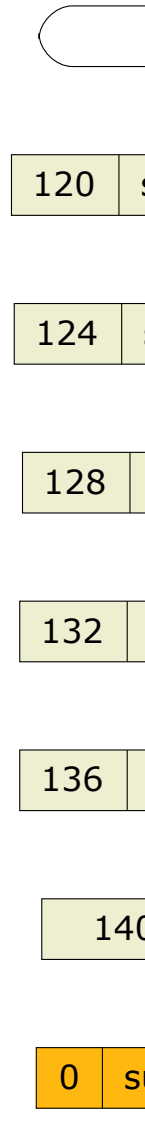

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 84:  e58d3004    str   r3, [sp, #4]
 88:  e59d0004    ldr   r0, [sp, #4]
 8c:  ebffffdb    bl    0 <fib>
 90:  e1a03000    mov   r3, r0
 94:  e1a00003    mov   r0, r3
 98:  e28dd00c    add   sp, sp, #12
 9c:  e49de004    pop   {lr}
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```
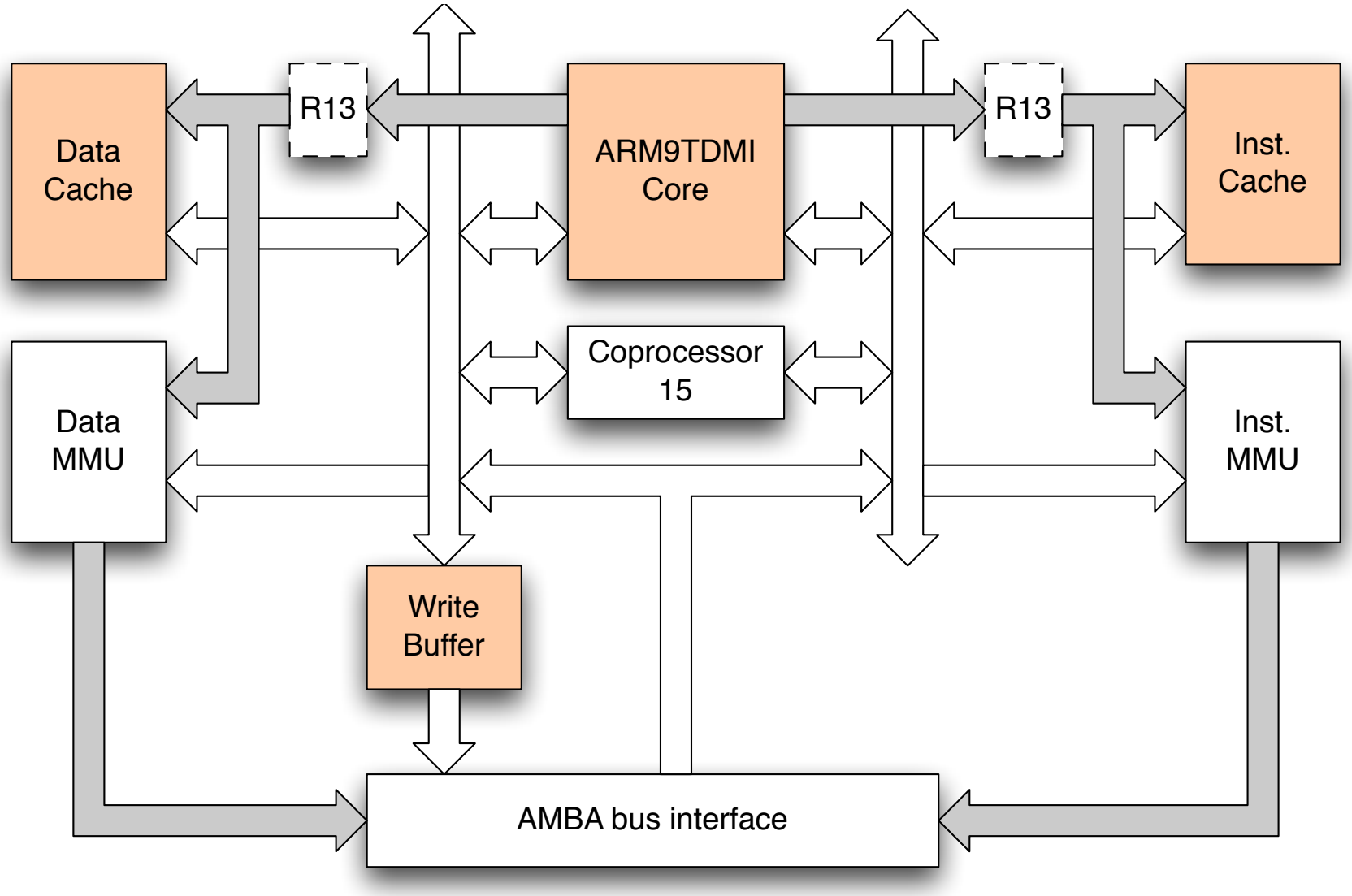
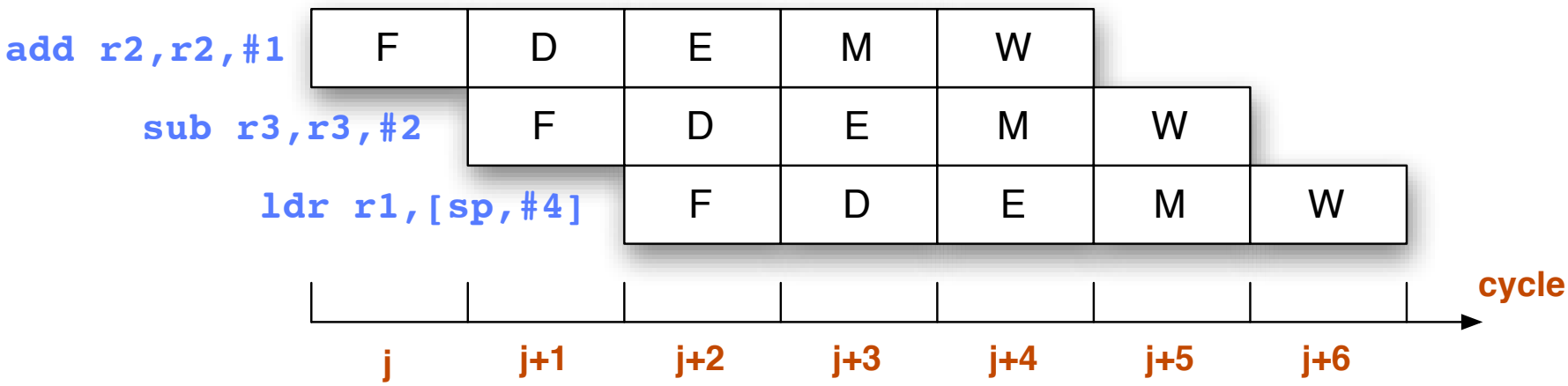

Target Architecture: ARM9xx family - ARM920T

- RISC processor, 16 registers, memory load/store and multiple ldr/str
- Data and Instruction Caches



Pipeline of the ARM920T

Pipelining = split execution of instructions into simple stages



Concurrent execution of stages : on average one cycle per instruction

. . . but sometimes pipeline stalls

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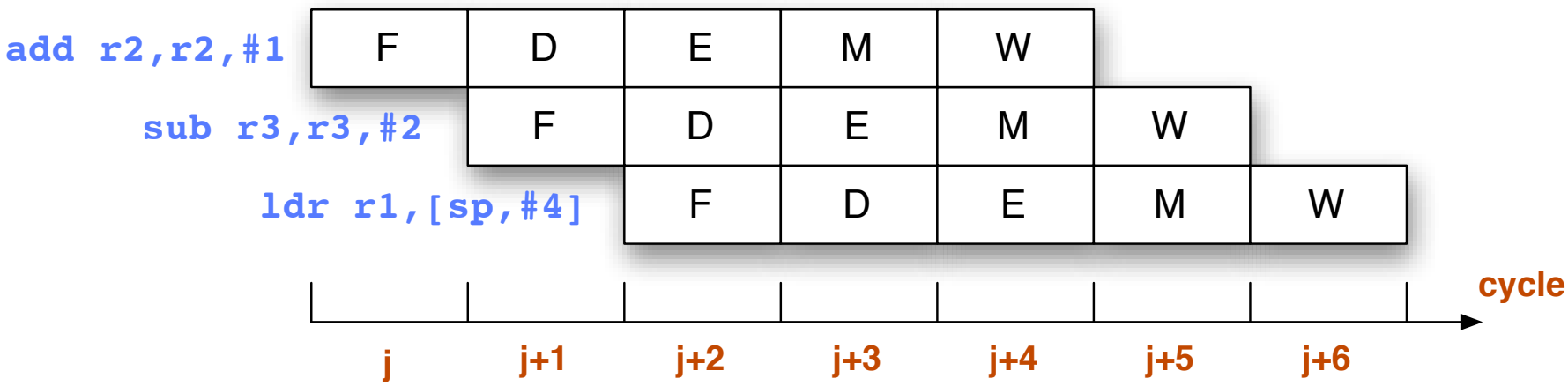

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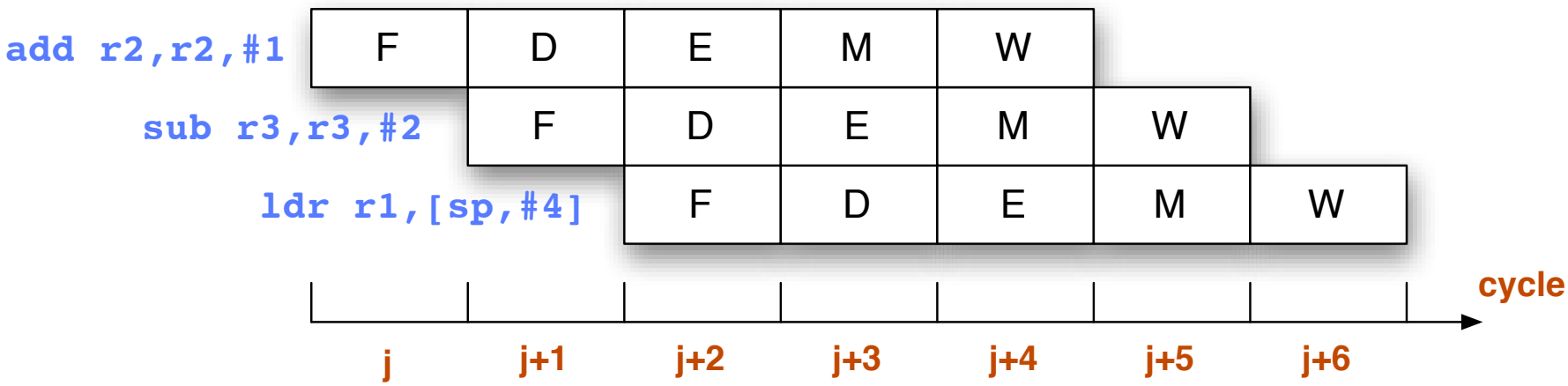

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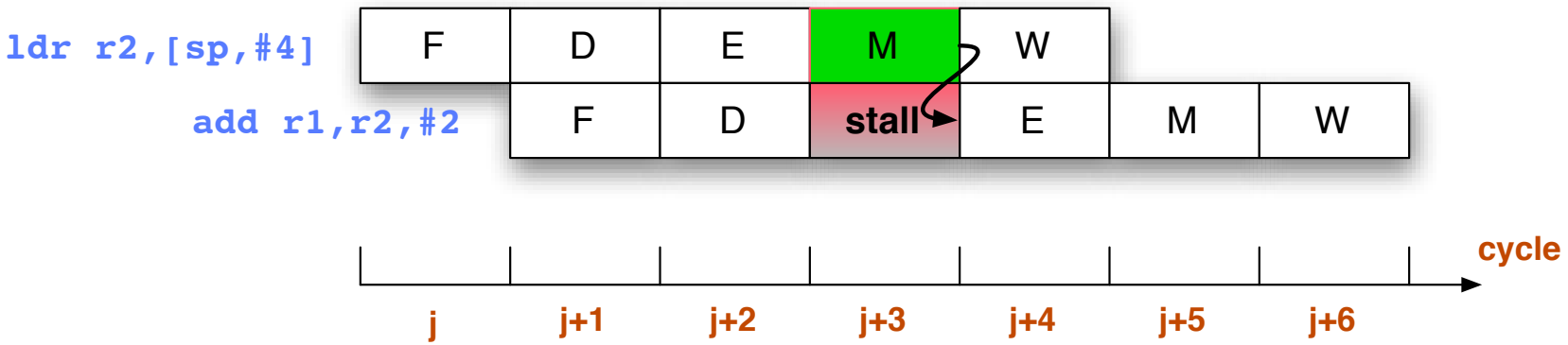
Pipeline Stalls

- Data dependences between instructions



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Summary:

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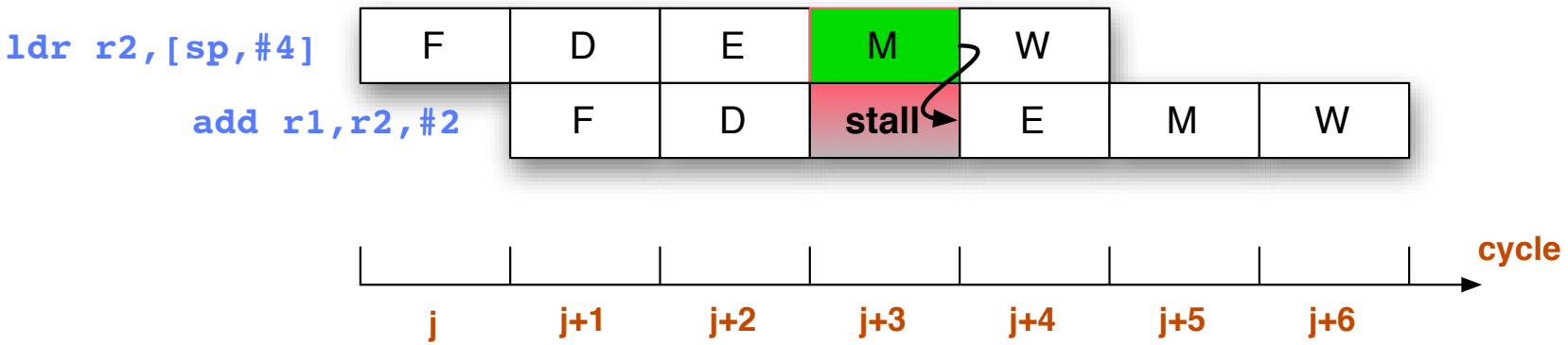

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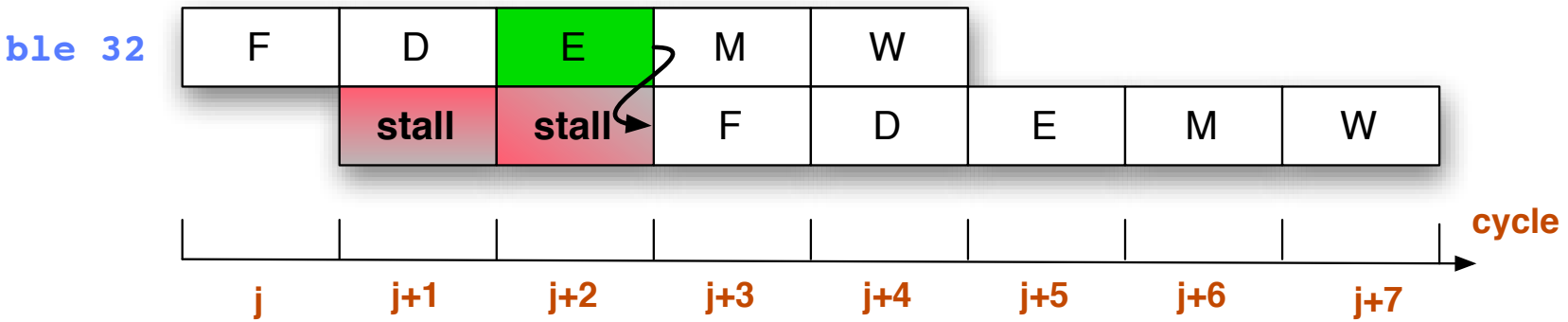

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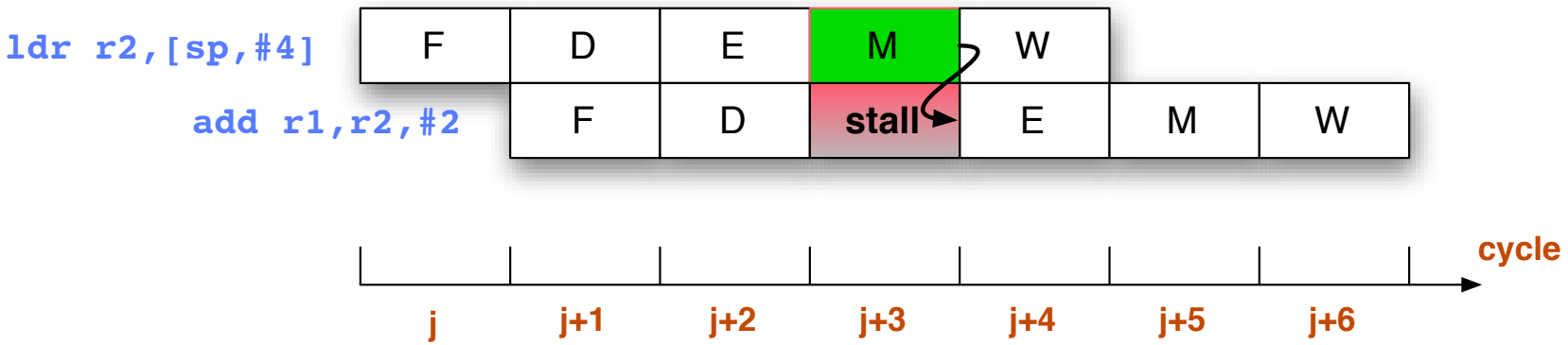

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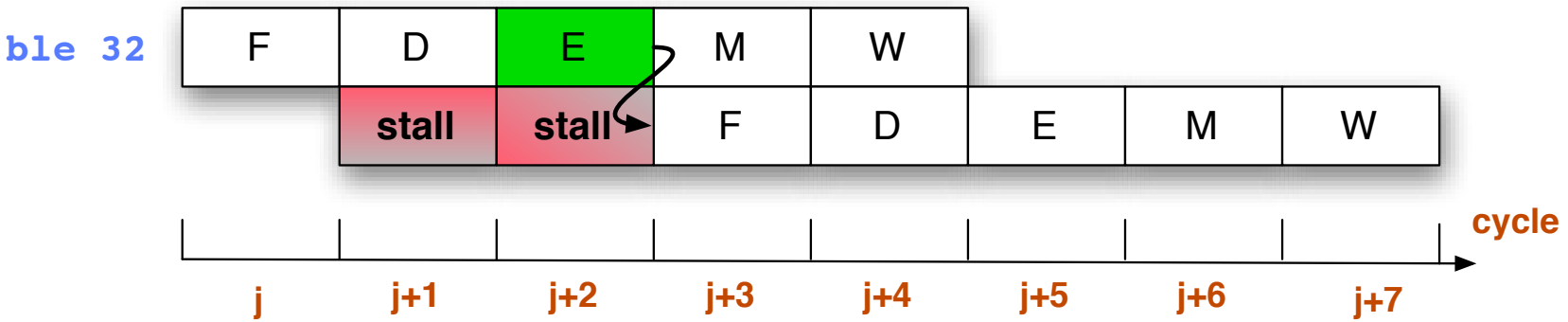

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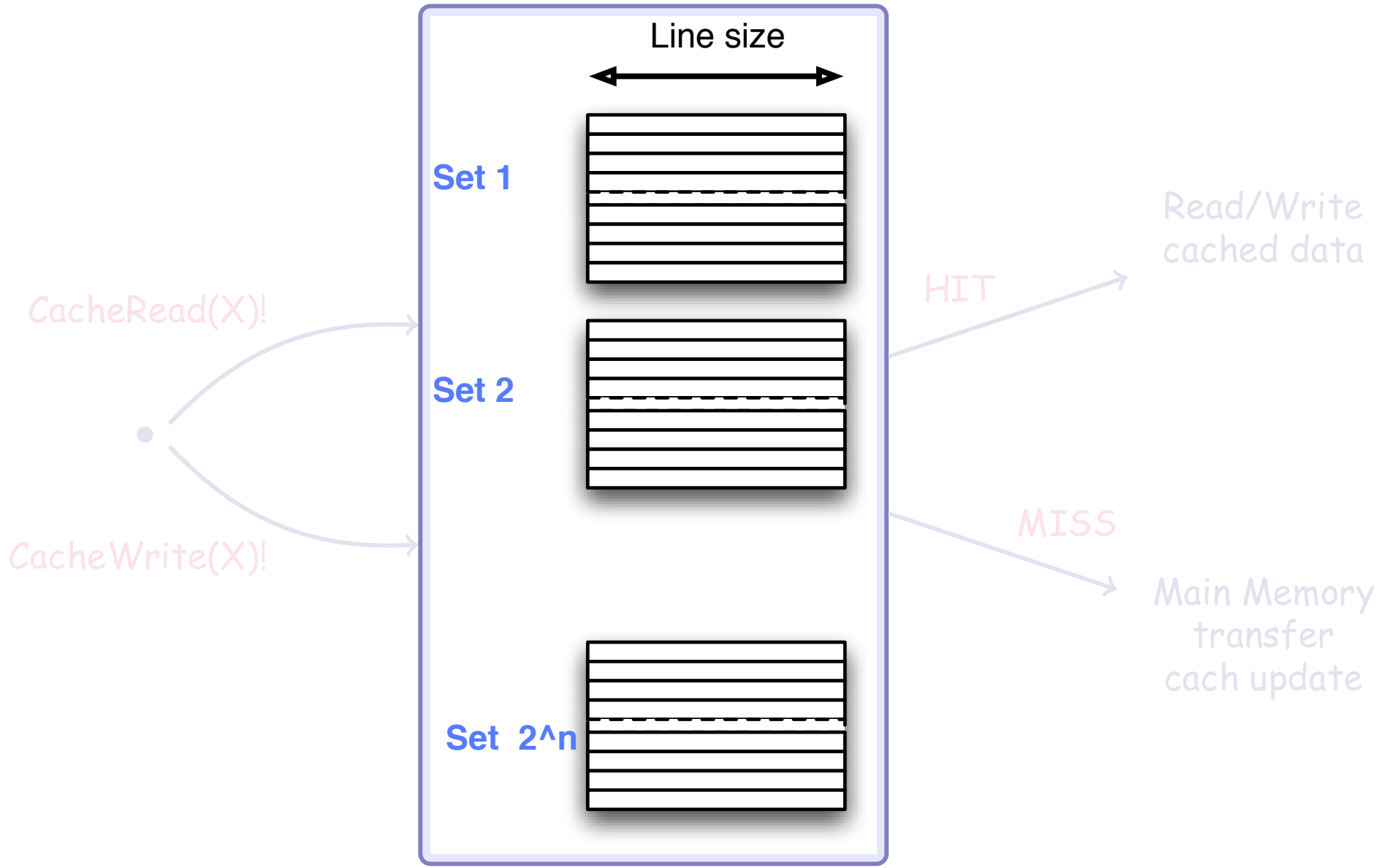
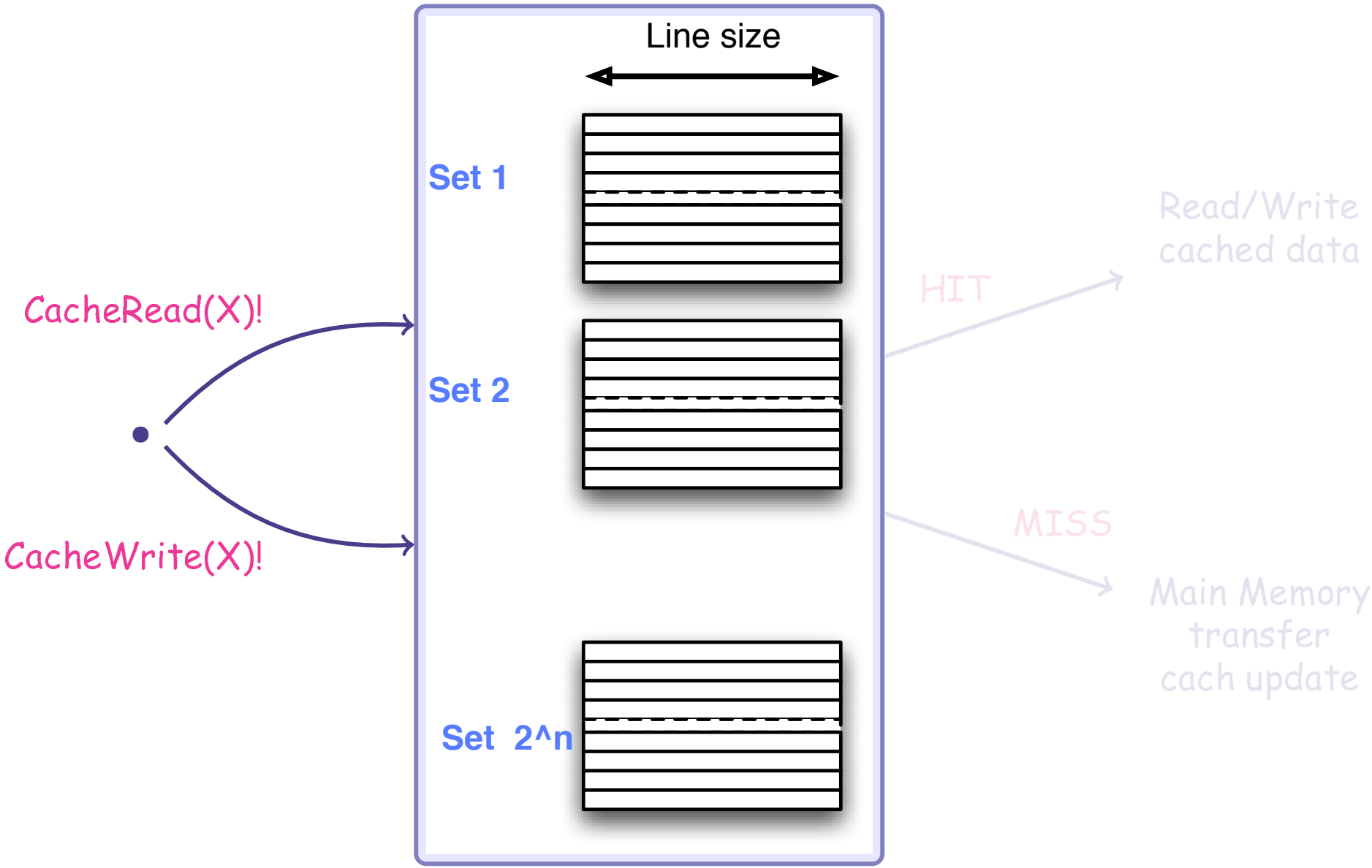

Line size
Set 1
Set 2
Set 2^n
CacheRead(X)!
CacheWrite(X)!
HIT
MISS
Read/Write
cached data
Main Memory
transfer
cach update

Caches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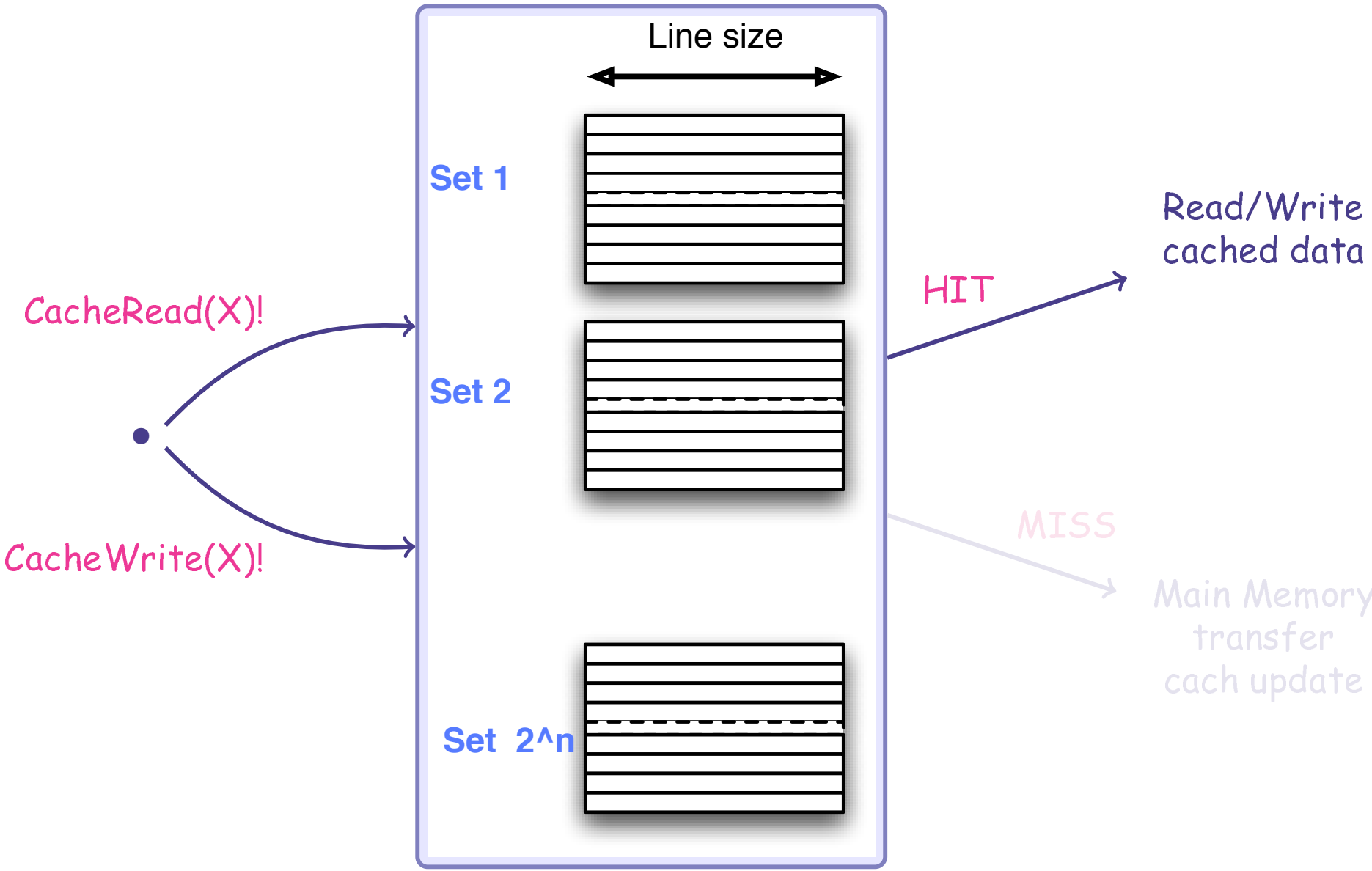
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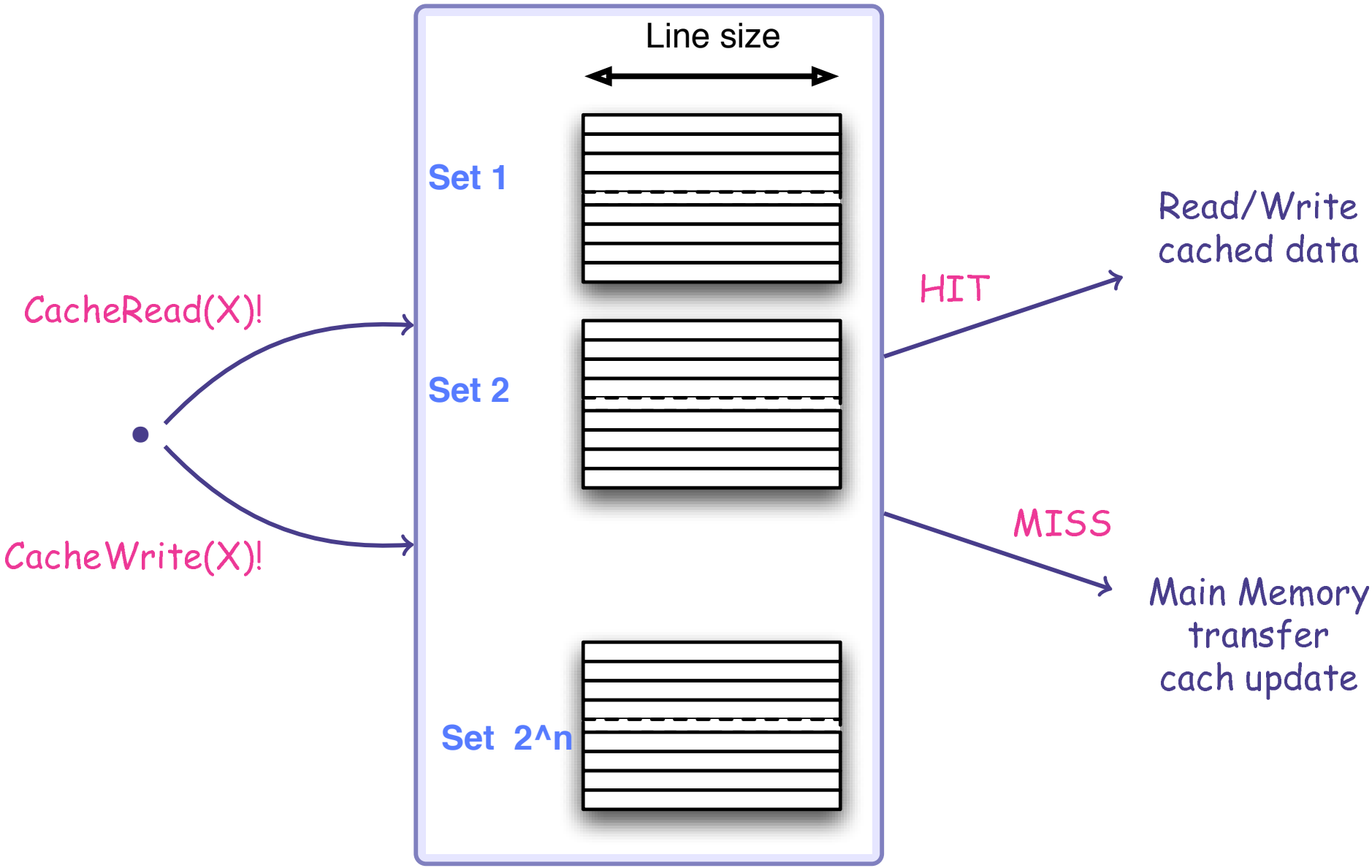
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What is really needed to compute WCET ?

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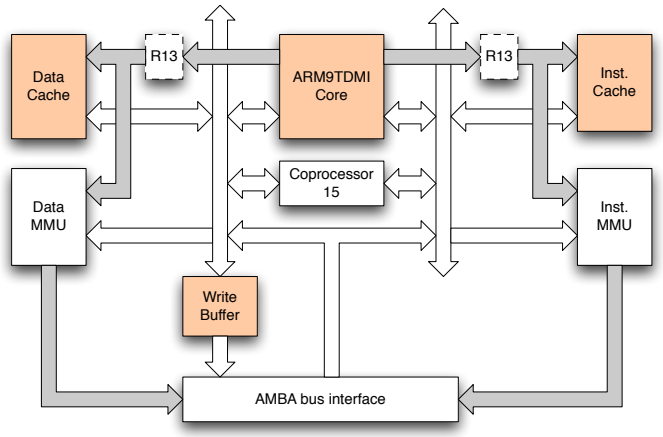

$\mathcal{L}(P) \subseteq \Sigma^*$

$\Sigma^* \longrightarrow \mathbb{N}$

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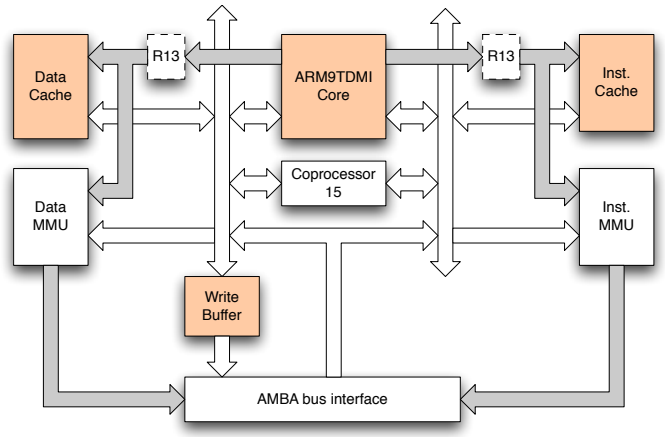

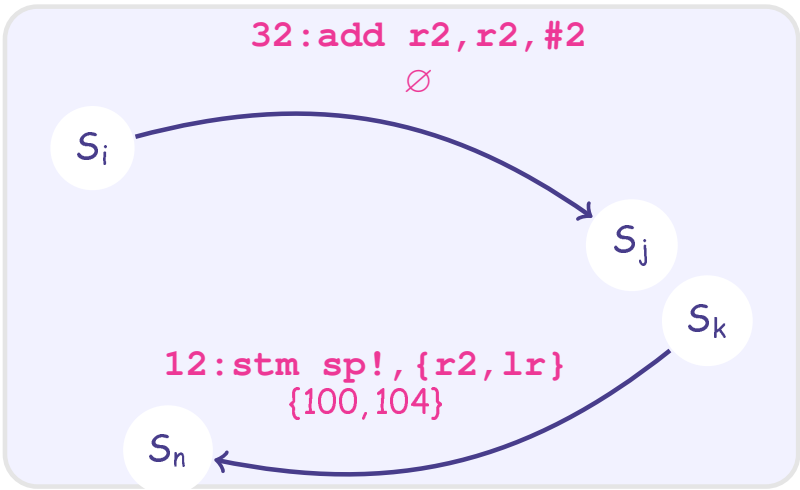

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What is really needed to compute WCET ?

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10:  e3a03000    mov   r3, #0
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18:  e3a03002    mov   r3, #2
1c:  e58d300c    str   r3, [sp, #12]
20:  ea00000a    b     50 <fib+0x50>
24:  e59d3010    ldr   r3, [sp, #16]
28:  e58d3018    str   r3, [sp, #24]
2c:  e59d2010    ldr   r2, [sp, #16]
30:  e59d3014    ldr   r3, [sp, #20]
34:  e0823003    add   r3, r2, r3
38:  e58d3010    str   r3, [sp, #16]
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40:  e58d3014    str   r3, [sp, #20]
44:  e59d300c    ldr   r3, [sp, #12]
48:  e2833001    add   r3, r3, #1
4c:  e58d300c    str   r3, [sp, #12]
50:  e59d200c    ldr   r2, [sp, #12]
54:  e59d3004    ldr   r3, [sp, #4]
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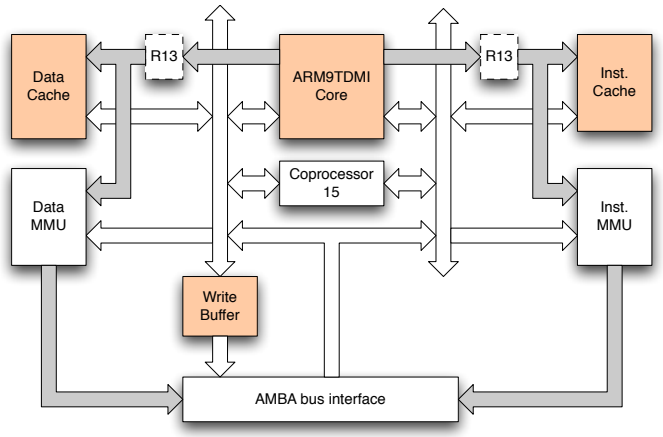

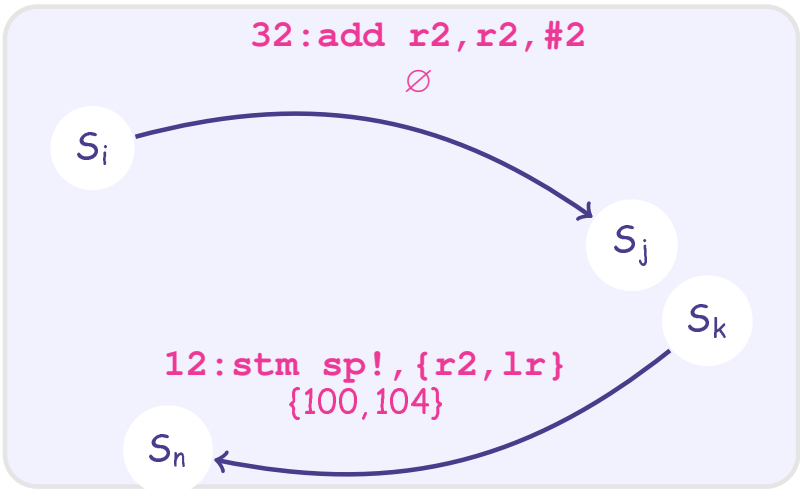

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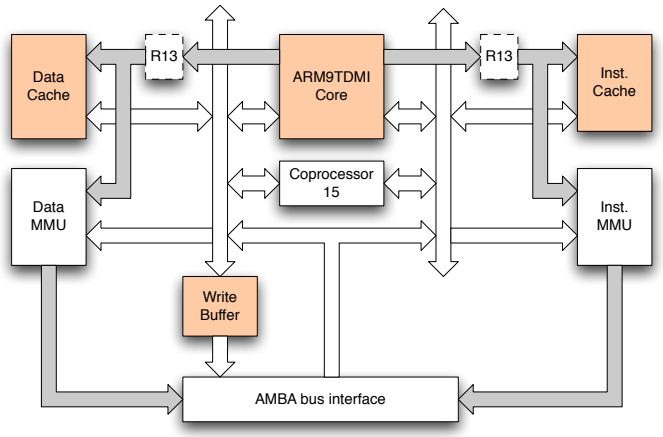

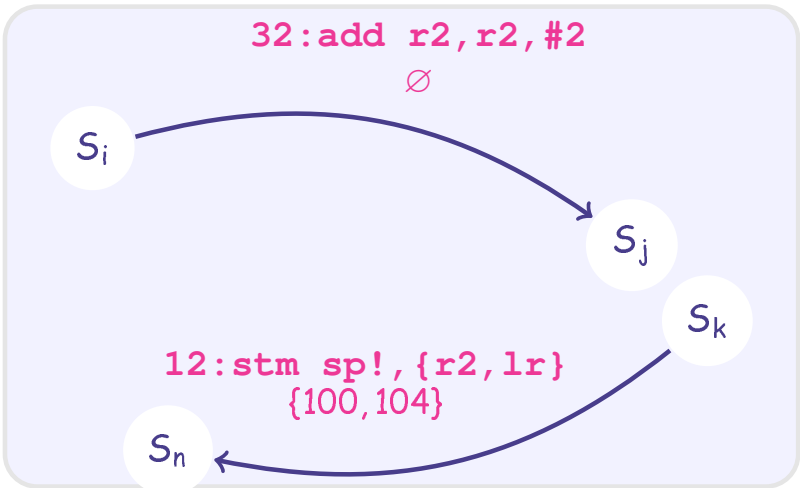

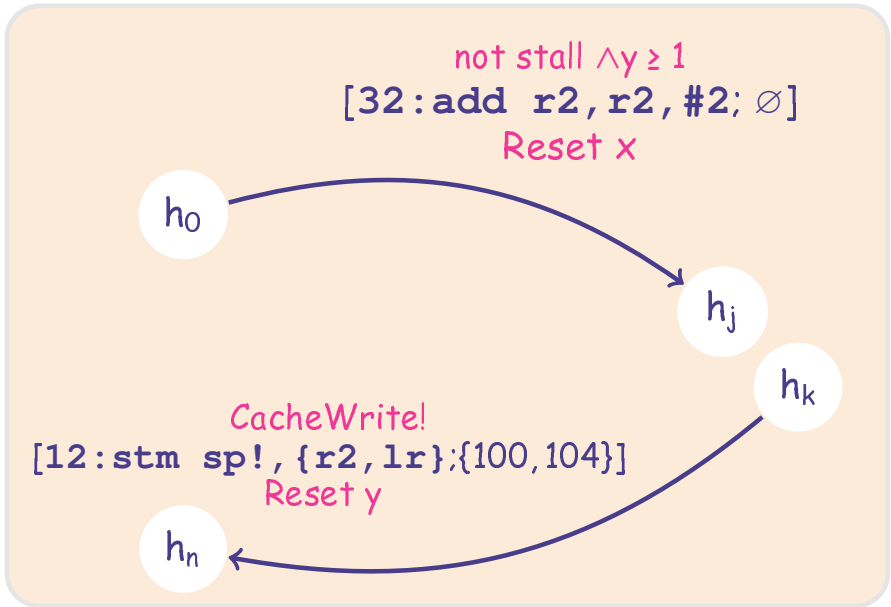

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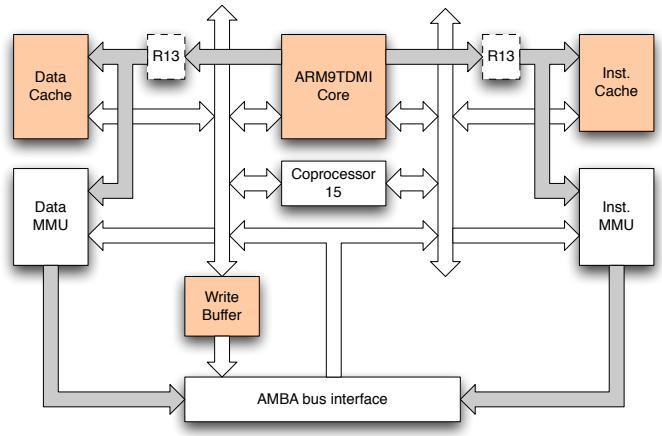

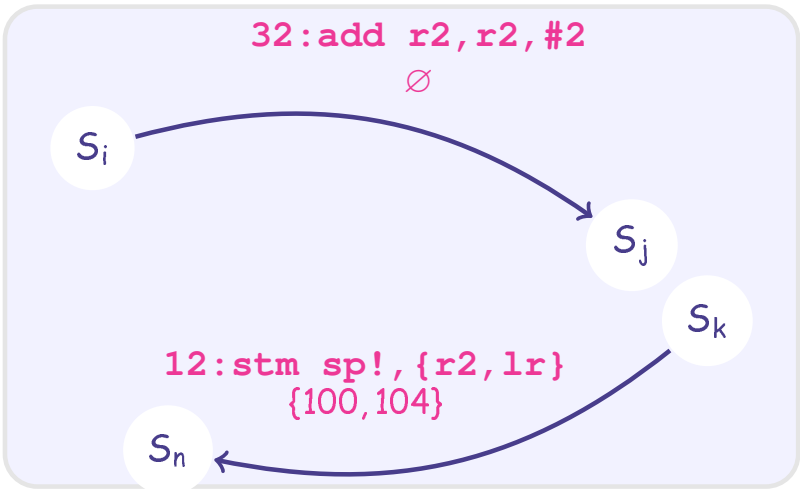

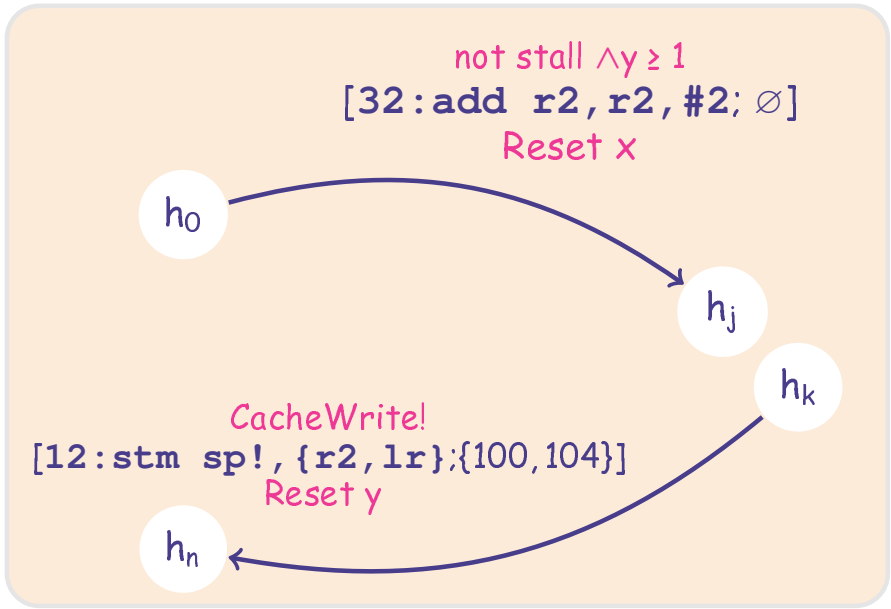

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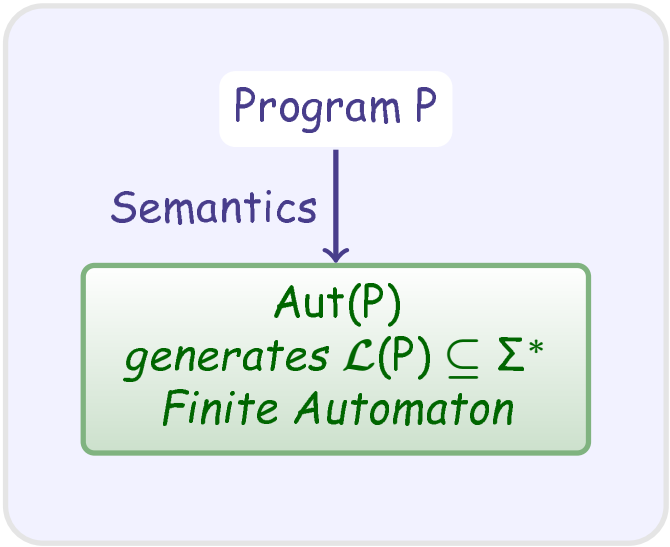
Modular Computation of WCET



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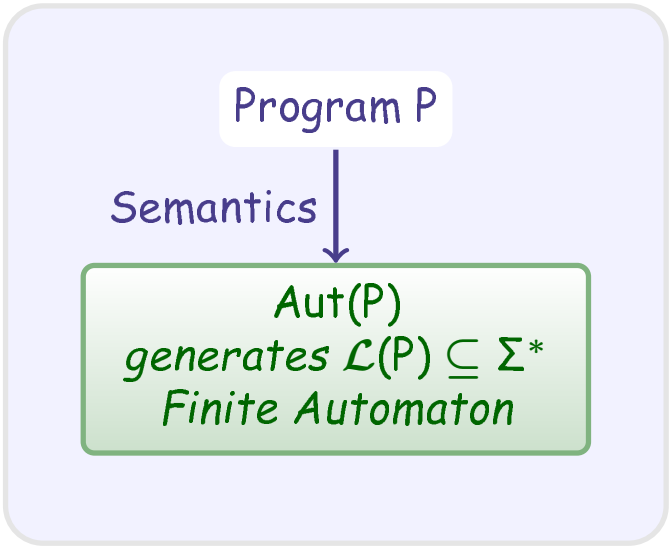

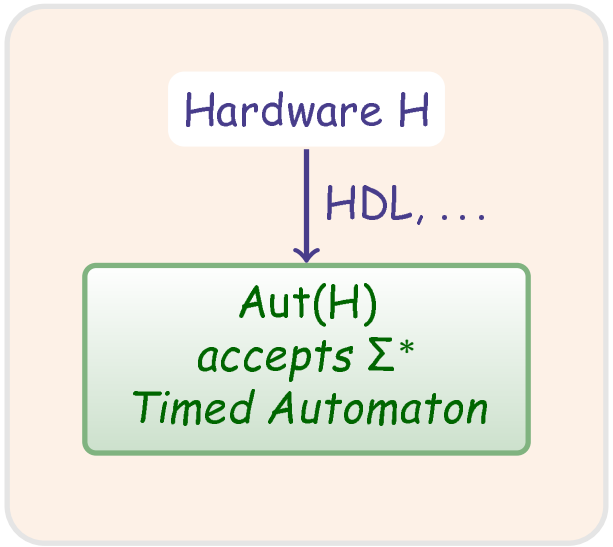

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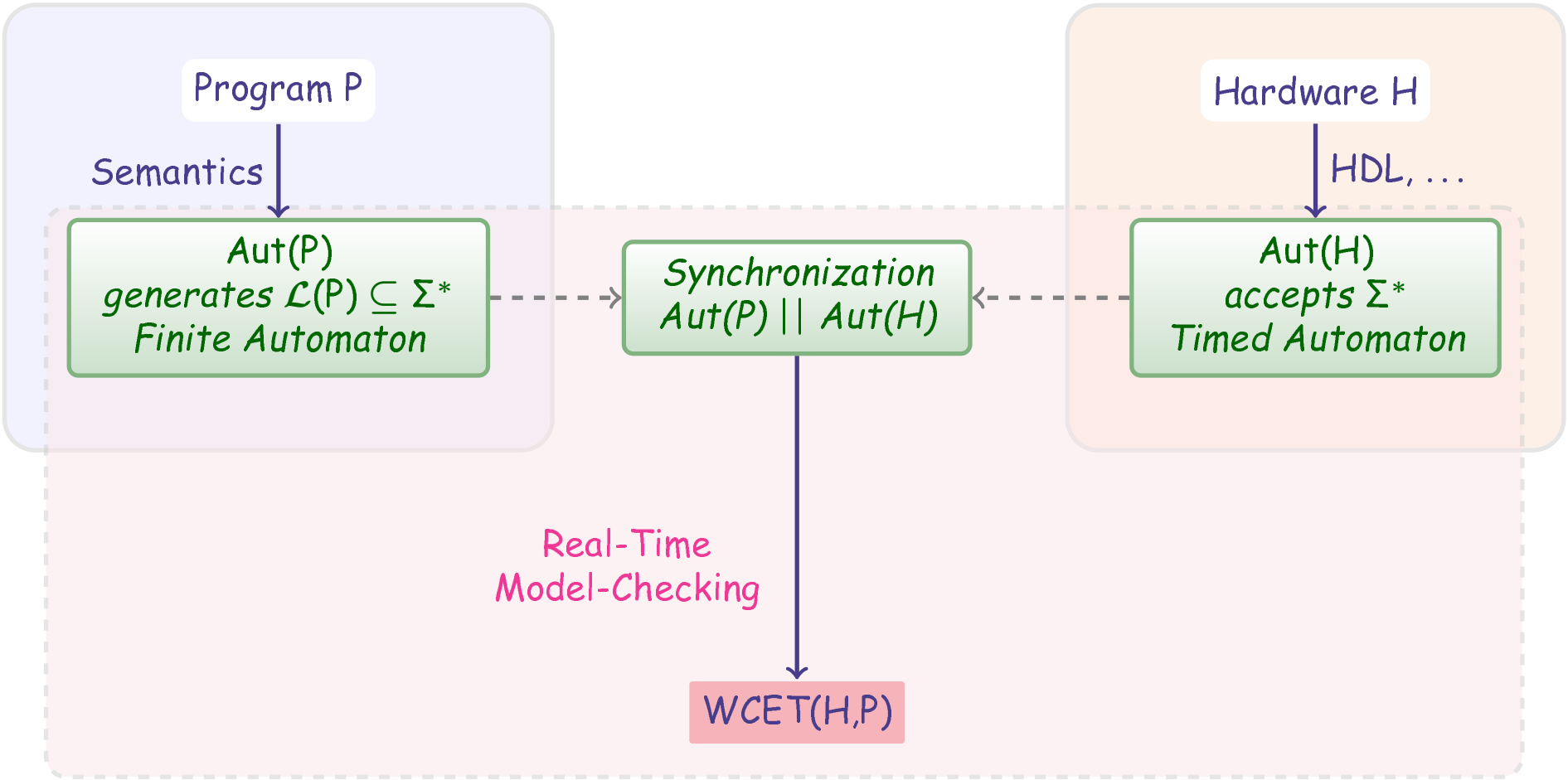

WCET-Equivalent Reduced Program

- Two runs of P can generate the same word in $\mathcal{L}(P)$
  e.g., Fibonacci with initial values $u_0 = 0, u_1 = 1$ and $u_0 = 2, u_1 = 3$
- state of Aut(P): 16 32-bit registers, stack, status bits
  size of a state of Aut(P): $16 \times 32 + |\text{stack}| \times 32 + 4$
- WCET depends on $\mathcal{L}(P)$

$$\text{if } \mathcal{L}(P') = \mathcal{L}(P) \text{ then } \text{WCET}(H, P) = \text{WCET}(H, P')$$

WCET-equivalent Program
P′ and P are WCET-equivalent iff $\mathcal{L}(P') = \mathcal{L}(P)$.

Compute a reduced WCET-equivalent P′ using Program Slicing

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Sliced Fibonacci Program

{r0,r2,r3,stack_3020,stack_3028,stack_3052}

```
00000000 <fib>:
   0:  e24dd020     sub   sp, sp, #32
   4:  e58d0004     str   r0, [sp, #4]
   8:  e3a03001     mov   r3, #1
   c:  e58d3010     str   r3, [sp, #16]
  10:  e3a03000     mov   r3, #0
  14:  e58d3014     str   r3, [sp, #20]
  18:  e3a03002     mov   r3, #2          <-
  1c:  e58d300c     str   r3, [sp, #12]   <-
  20:  ea00000a     b     50 <fib+0x50>
  24:  e59d3010     ldr   r3, [sp, #16]
  28:  e58d3018     str   r3, [sp, #24]
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  40:  e58d3014     str   r3, [sp, #20]
  44:  e59d300c     ldr   r3, [sp, #12]   <-
  48:  e2833001     add   r3, r3, #1      <-
  4c:  e58d300c     str   r3, [sp, #12]   <-
  50:  e59d200c     ldr   r2, [sp, #12]   <-
  54:  e59d3004     ldr   r3, [sp, #4]    <-
  58:  e1520003     cmp   r2, r3          <-
  5c:  dafffff0     ble   24 <fib+0x24>   <-
  60:  e59d3010     ldr   r3, [sp, #16]
  64:  e58d301c     str   r3, [sp, #28]
  68:  e59d301c     ldr   r3, [sp, #28]
  6c:  e1a00003     mov   r0, r3
  70:  e28dd020     add   sp, sp, #32
  74:  e12fff1e     bx    lr

00000078 <main>:
  78:  e52de004     push  {lr}
  7c:  e24dd00c     sub   sp, sp, #12
  80:  e3a03f4b     mov   r3, #300        <-
  84:  e58d3004     str   r3, [sp, #4]    <-
  88:  e59d0004     ldr   r0, [sp, #4]    <-
  8c:  ebffffdb     bl    0 <fib>
  90:  e1a03000     mov   r3, r0
  94:  e1a00003     mov   r0, r3
  98:  e28dd00c     add   sp, sp, #12
  9c:  e49de004     pop   {lr}
  a0:  e12fff1e     bx    lr
```
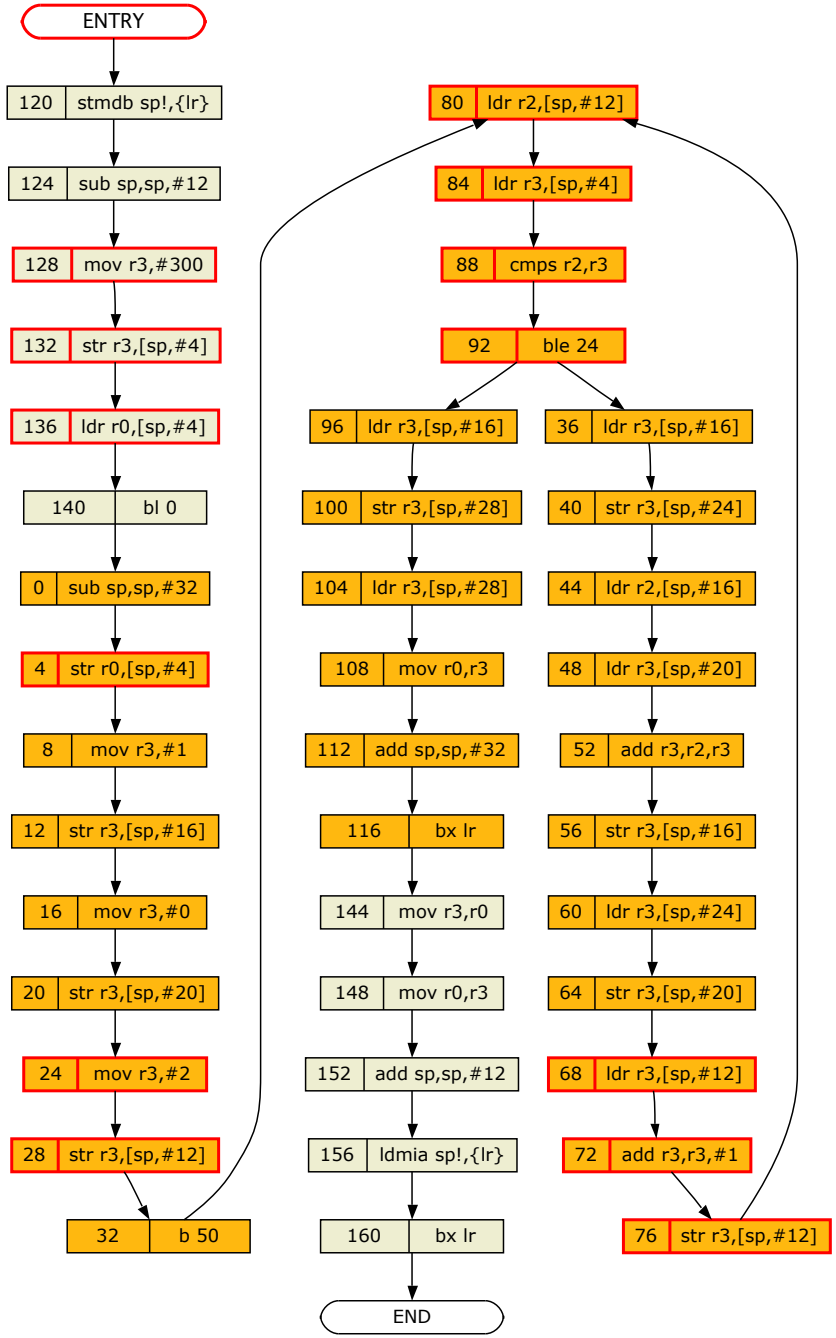
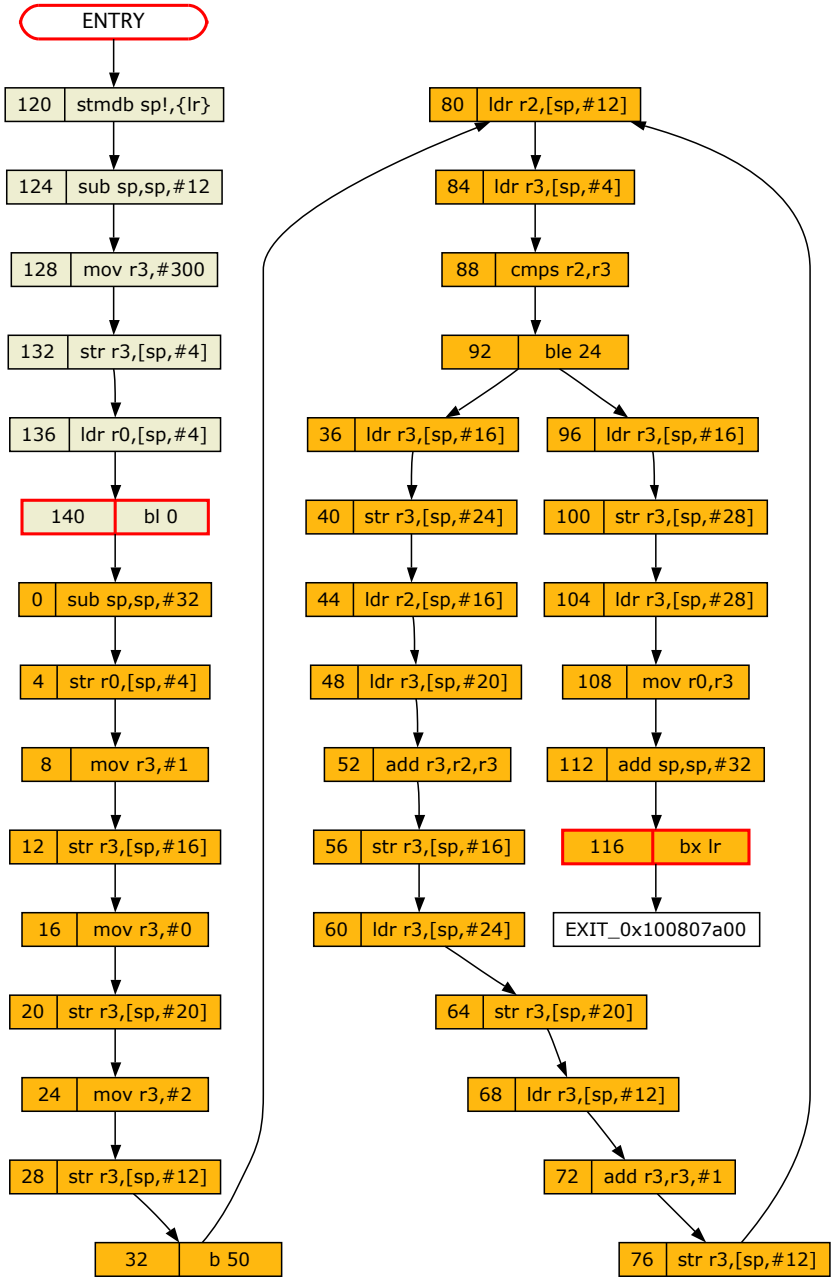



Automatic Computation of CFG using Program Slicing



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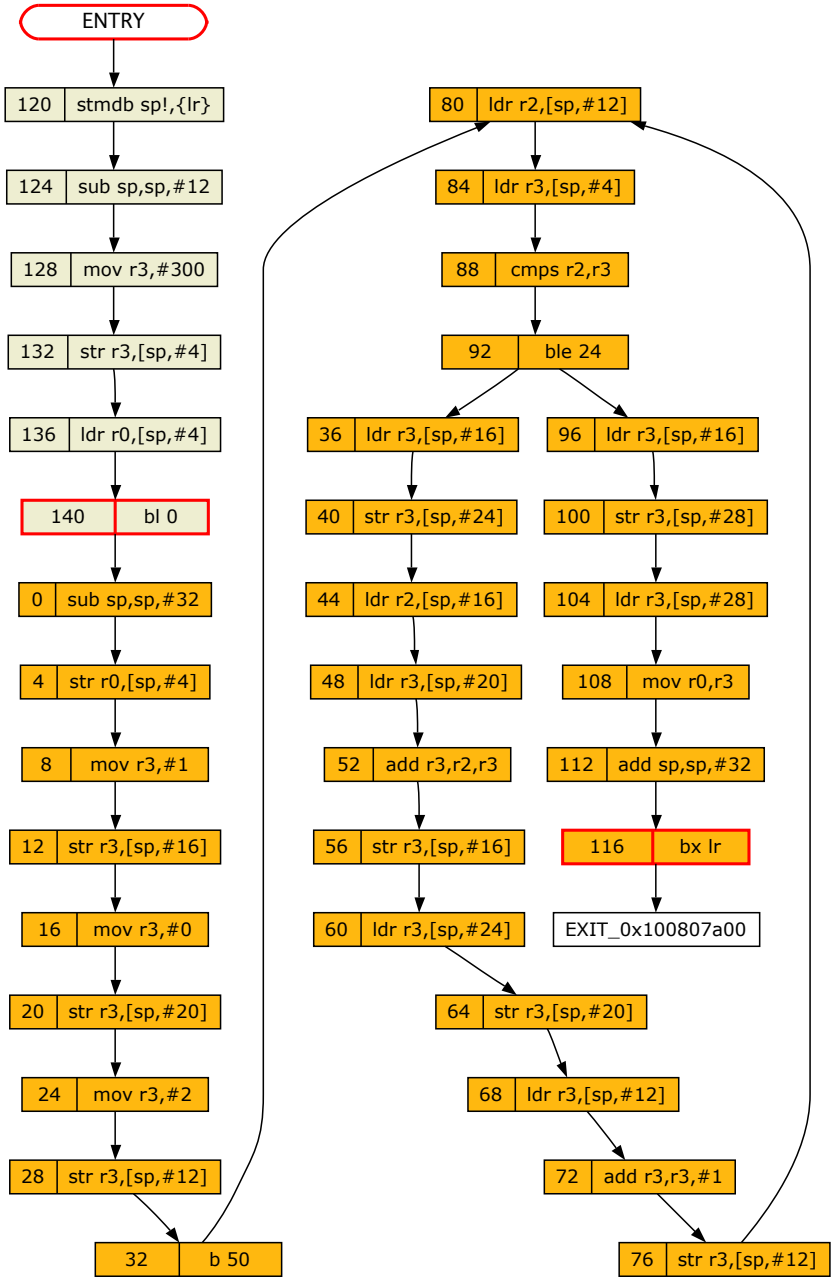
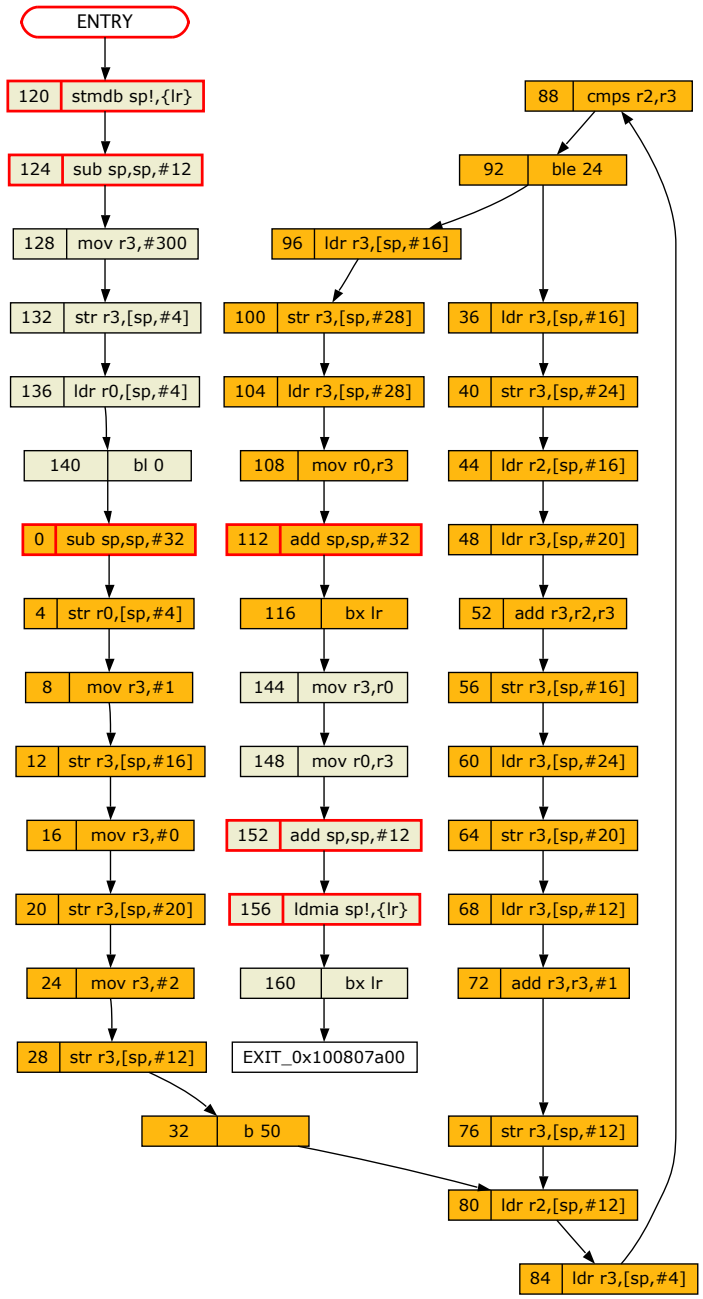
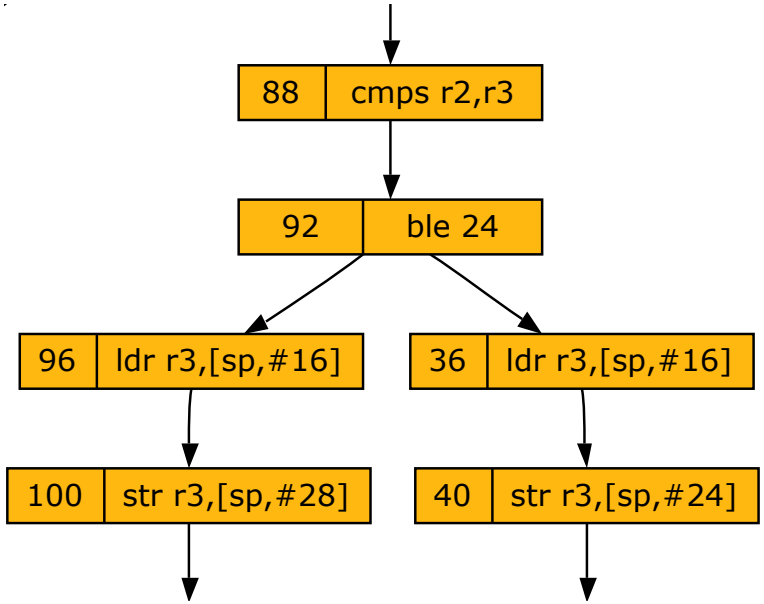
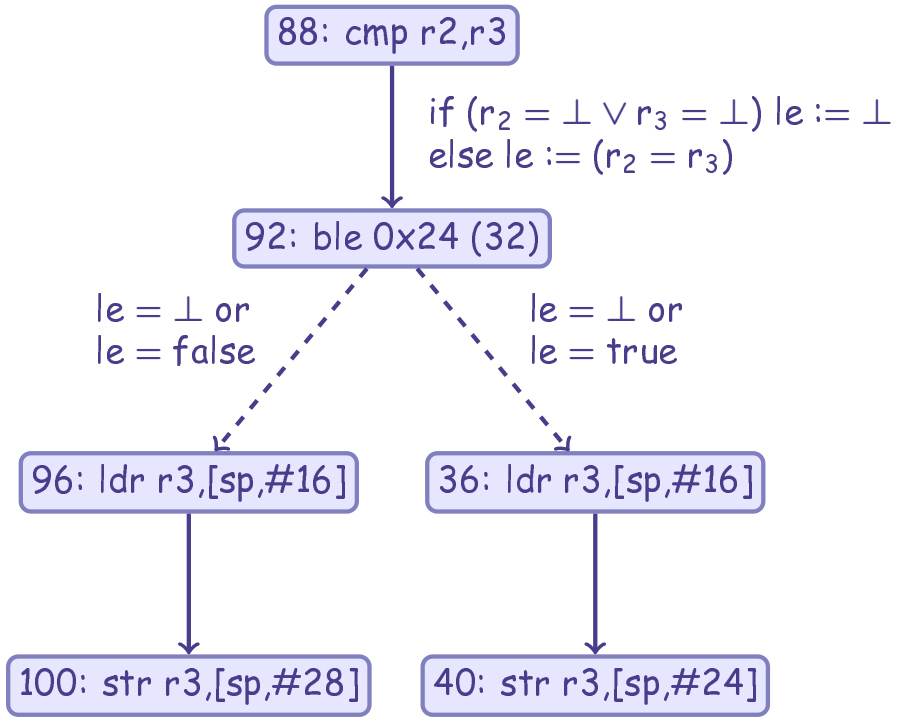




Handling Unknown Input Data

Input data are unknown: extended domain: $\mathcal{D}_\perp = \mathcal{D} \cup \{\perp\}$





Game: program vs outcomes of comparisons

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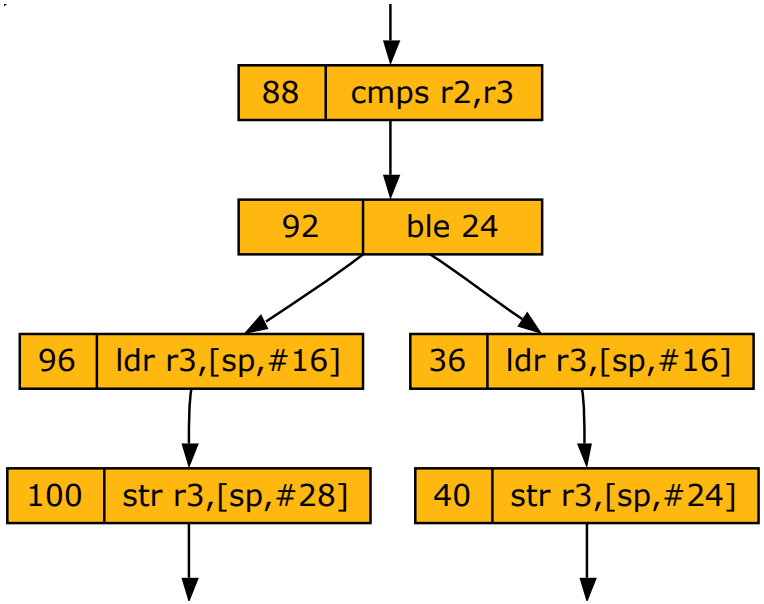

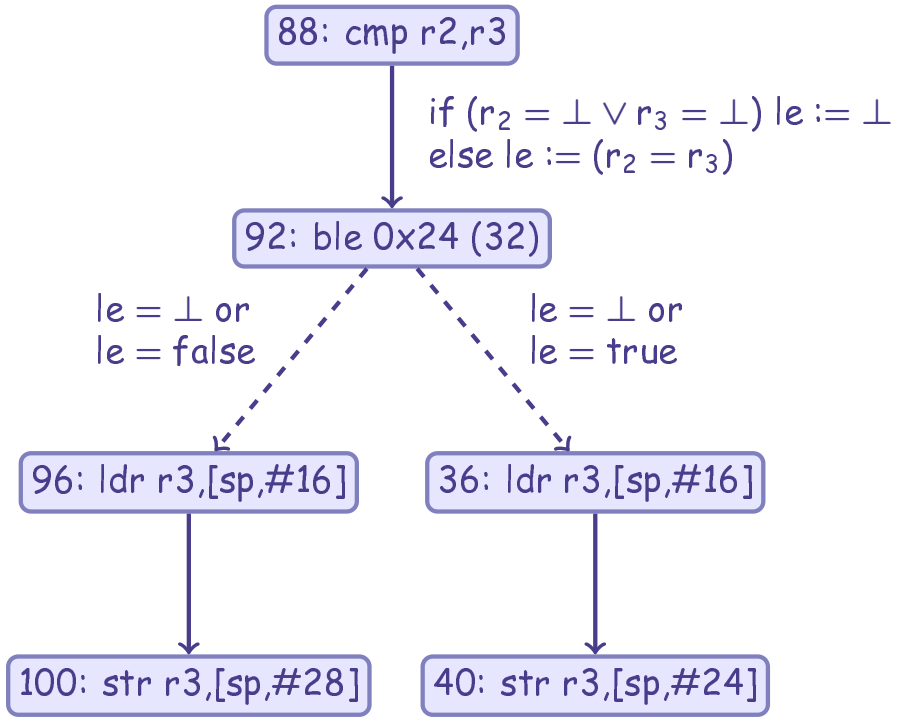

Game: program vs outcomes of comparisons

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Formal Models

- Timed Automata: automata extended with dense-time clocks

Hardware Specs ?

- Data sheets
- Incomplete or sketchy

Bad formal models $\Longrightarrow$ very bad WCET results

How can we build better models ?

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- Design programs to stress particular features of the hardware
- Compare actual execution-times with computed execution-times
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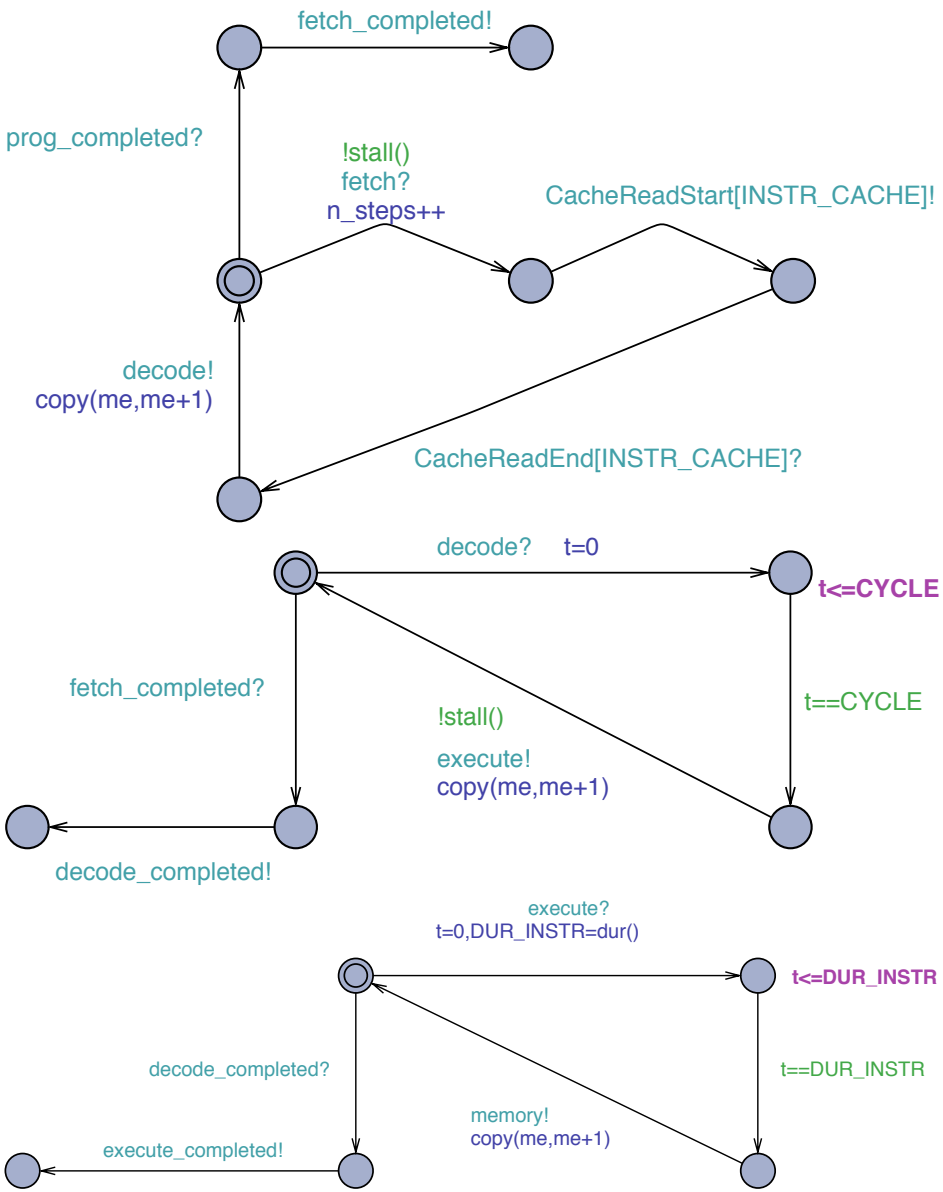
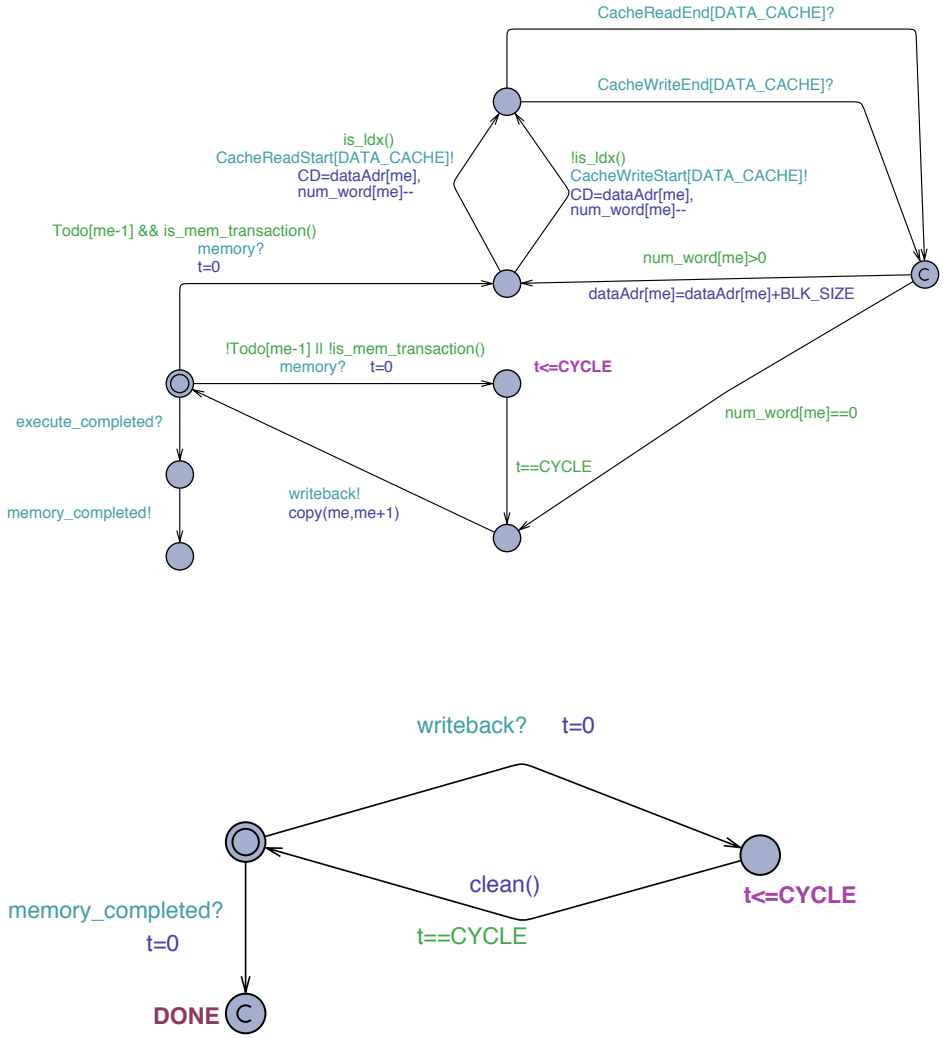
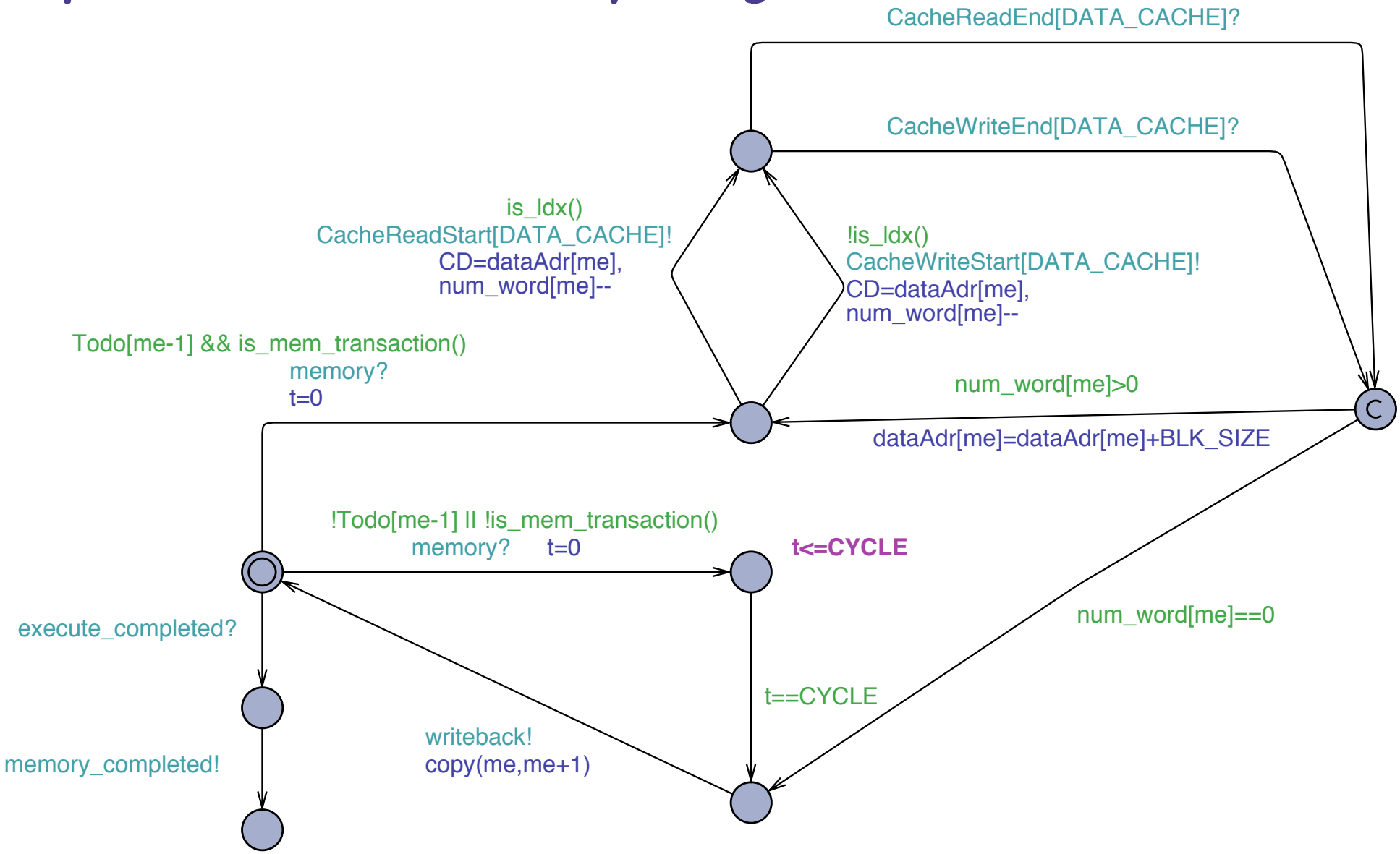
Pipeline Model

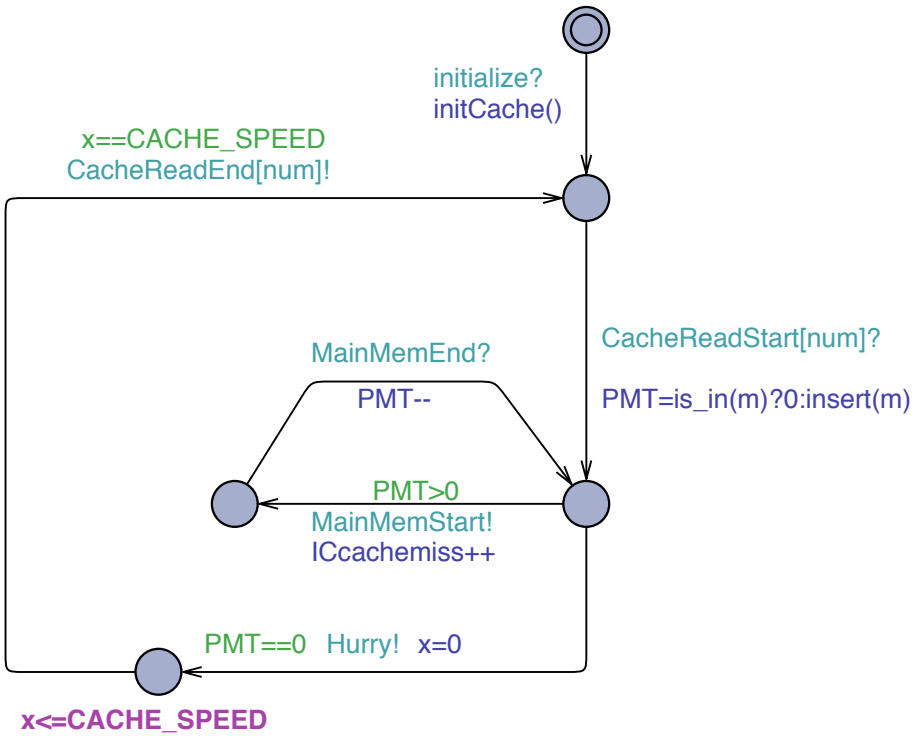


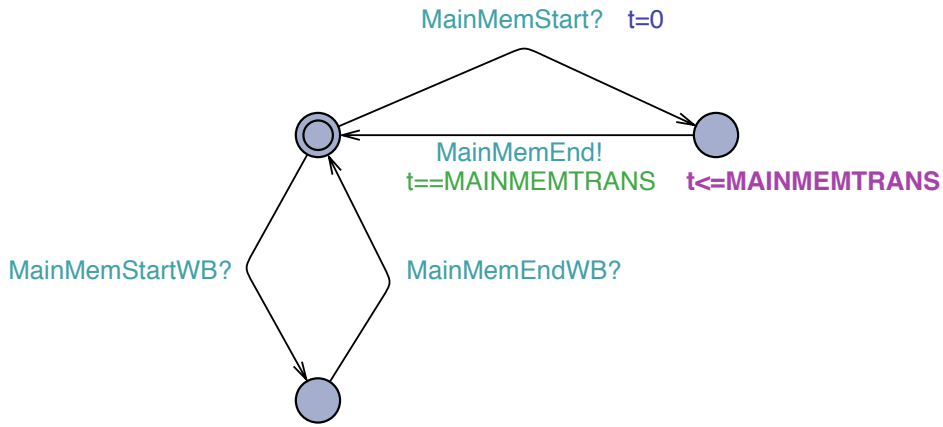


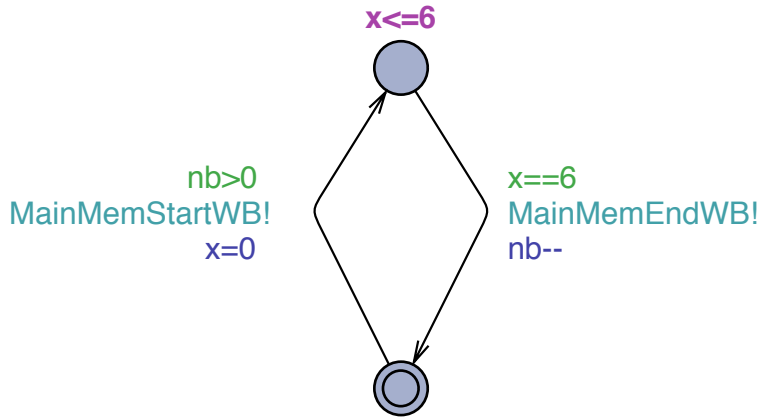
Pipeline Model – Memory Stage



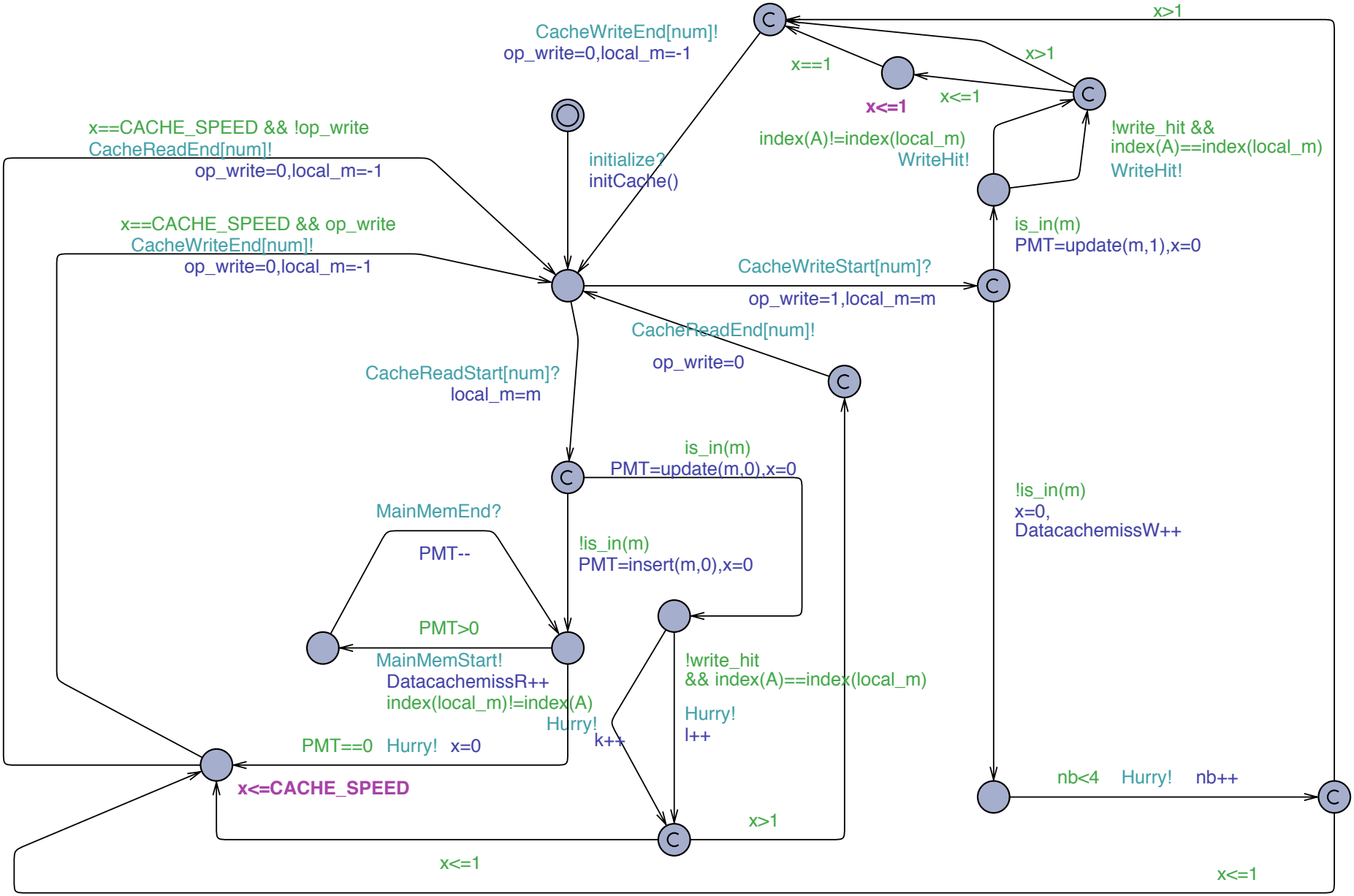
Instruction Cache & Main Memory



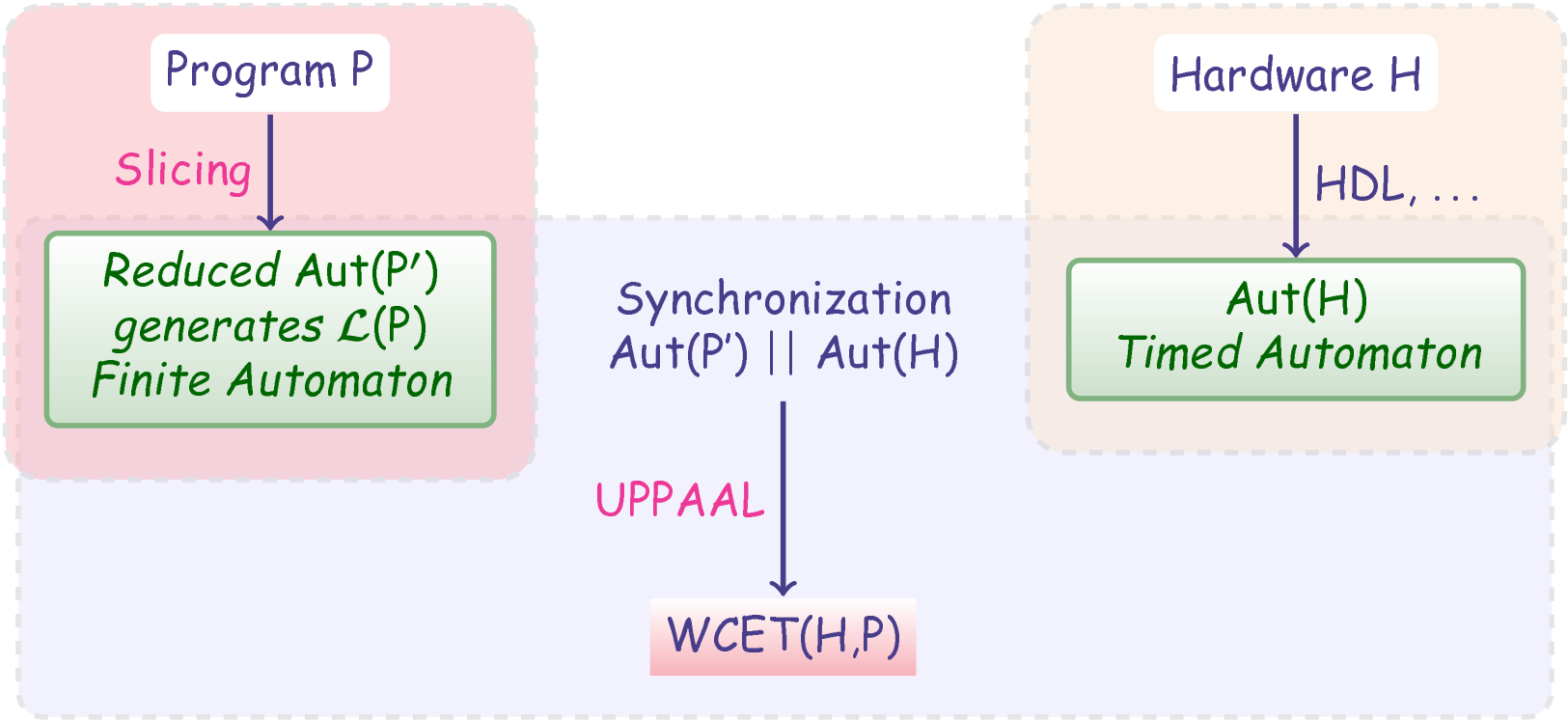




Data Cache


x>1
CacheWriteEnd[num]!
op_write=0,local_m=-1
x==1
x>1
x<=1
x<=1
x==CACHE_SPEED && !op_write
CacheReadEnd[num]!
op_write=0,local_m=-1
initialize?
initCache()
index(A)!=index(local_m)
WriteHit!
!write_hit &&
index(A)==index(local_m)
WriteHit!
x==CACHE_SPEED && op_write
CacheWriteEnd[num]!
op_write=0,local_m=-1
is_in(m)
PMT=update(m,1),x=0
CacheWriteStart[num]?
op_write=1,local_m=m
CacheReadEnd[num]!
op_write=0
CacheReadStart[num]?
local_m=m
is_in(m)
PMT=update(m,0),x=0
!is_in(m)
x=0,
DatacachemissW++
MainMemEnd?
PMT--
!is_in(m)
PMT=insert(m,0),x=0
PMT>0
MainMemStart!
DatacachemissR++
index(local_m)!=index(A)
Hurry!
k++
!write_hit
&& index(A)==index(local_m)
Hurry!
l++
PMT==0 Hurry! x=0
x<=CACHE_SPEED
nb<4 Hurry! nb++
x>1
x<=1
x<=1

Tool Chain



Slicing

[Tarjan, 1979] Thomas Lengauer and Robert Endre Tarjan.
A fast algorithm for finding dominators in a flowgraph.
ACM Trans. Program. Lang. Syst., 1(1):121–141, 1979.

Real-Time Model-Checking

[UPPAAL] K. G. Larsen, P. Pettersson, and W. Yi.
UPPAAL **in a Nutshell.**
Journal of Software Tools for Technology Transfer (STTT), 1(1-2):134–152, 1997.

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- Formal models of hardware (pipeline and caches)
  Identification of hardware features
- Computation of WCET as a reachability property
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Experiments to evaluate tightness of results

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New Features

- Processor speed changes
- For OS programs, model for interruptions' arrivals

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- Compute a witness trace that gives the WCET
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Is Slicing Critical ?

METAMOC [Master's Thesis 2009, WCET'2010]

- Mälardalen University Sweden and Aalborg Univ. Denmark
- Timed automata (hardware model)
- Annotate with loop bounds
- Value analysis phase
- Loop unfolding
- Compute WCET using UPPAAL

Results (from **http://metamoc.dk/**)

- Programs compiled with O2 option
- Simple cache formal models

Is Slicing Critical ?

WCET2010 - LRU

	ATMEL	ARM9	ARM9	ARM9	ARM9	ARM9	ARM9
Optimization	O2	O2	O2	O2	O2	O2	O2
Data-cache	-	miss_writeback	miss_writeback	miss_writeback	Concrete, 64 lines/set, LRU	Concrete, 128 lines/set, LRU	Concrete, LRU
Instr.-cache	-	miss	Concrete, 128 lines/set, LRU	Concrete, LRU	Concrete, LRU	Concrete, LRU	Concrete, LRU
Value-analysis	No	No	No	No	Yes	Yes	Yes
adpcm	**OOM**	**19829472**		**OOM/error**			**OOM/error**
	1:44:19	20:12.95		1:46.67			4:44.83
bs	**146**	**3666**		**964**			**640**
	0:03.66	0:01.09		0:01.06			0:01.27
bsort100		**7997421**		**3425868**	**408715**	**OOM**	**OOM/error**
		0:29.54		0:57.66	2:06.05	2:02.95	1:50.13
cnt	**29572**	**188466**		**52481**			**6137**
	0:02.46	0:02.06		0:02.62			0:04.00
compress	**58352**	**158697**		**69488**		**Model invalid, manual mod.**	**60351**
	6:29.88	0:06.52		0:09.11		0:04.56+0:22.65	0:27.21
crc	**170959**	**2043591**		**328310**			**310722**
	0:36.71	0:13.42		0:26.32			0:39.83
edn	**345499**	**2093937**		**687463**			**431334**
	0:29.42	0:12.81		0:20.56			4:20.71
expint	**7583931**	**652215**		**31483**			**30577**
	4:56.17	0:04.33		0:08.75			0:12.72
fac	**906**	**11553**		**1266**			**683**
	0:01.43	0:01.05		0:01.02			0:01.35
fdct	**4806**	**344234**		**190692**			**168827**
	0:02.43	0:07.10		0:08.26			41:22.70
fibcall	**438**	**13434**		**632**			**599**
	0:01.04	0:01.09		0:01.08			0:01.52
fir	**782494**	**131508**		**21364**			**18763**
	0:25.90	0:02.02		0:02.73			0:04.53
insertsort	**2872**	**75078**		**43888**			**37814**
	0:01.26	0:01.20		0:01.31			0:02.44
janne_complex	**OOM**	**57787**		**1883**			**1883**
	2:11:27	0:01.17		0:01.33			0:01.92
jfdctint	**54383**	**294957**		**133059**			**111510**
	0:05.80	0:05.39		0:06.41			16:46.68
matmult	**525383**	**5836449**		**2636715**		**712869**	**OOM/error**
	0:17.02	0:22.16		0:40.72		1:28.47	1:36.94
ndes	**OOM**	**2575484**	**1084016**	**OOM/error**			**OOM/error**
	26:47.04	2:55.38	7:33.04	8:27.09			4:25.09
ns	**13116**	**279579**		**29060**			**10813**
	0:01.79	0:02.20		0:03.43			0:07.09
nsichneu		**1020957**		**622904**			**295997**
		3:04.11		3:25.56			3:37.70
prime	**170806**	**6477669**		**470372**			**469060**
	0:12.52	1:02.36		1:56.36			2:41.87
ud	**58217**	**1160049**		**175359**			**165814**
	0:11.81	0:07.76		0:14.64			0:23.07
	3 errors / 19 benchmarks	0 errors / 21 benchmar	1 errors / 21 benchmarks	errors / 21 benchmarks	2 errors / 21 benchmarks	3 errors / 21 benchmarks	4 errors / 21 benchmarks
	Model checking fails: 3		Model checking fails: 1 Manual modification: 1	Model checking fails: 2 Manual modification: 0	Value analysis fails: 0 Model checking fails: 2 Manual modification: 3	Value analysis fails: 0 Model checking fails: 3 Manual modification: 2	Value analysis fails: 0 Model checking fails: 4 Manual modification: 1

Program Slicing, M. Weiser [Weiser, 1984]

I = set of instructions in P

Slicing

- slice criterion: subset $I' \subseteq I$ and variables $\mathcal{V}(i)$ for each $i \in I'$
  `4:str r0,[sp,#4]` and variable `sp`
- Slice of P = sub-program P′ of P satisfying (1) and (2)
  - given input $d \in \mathcal{D}$,

    run of P on d $\quad \rho = (i_0, v_0)\ (i_1, v_1)\ \cdots\ (i_k, v_k)\ \cdots\ (i_n, v_n)$

    run of P′ on d $\quad \rho' = (i'_0, v'_0)\ (i'_1, v'_1)\ \cdots\ (i'_l, v'_l)\ \cdots\ (i'_m, v'_m)$

  - projection: for a pair (i, v), $\mathrm{proj}(i, v) = \begin{cases} \varepsilon \text{ if } i \notin I' \\ (i, \mathrm{proj}_{\mathcal{V}(i)}(v)) \text{ otherwise} \end{cases}$
  - for sequences of pairs: $\mathrm{proj}^*(\varepsilon) = \varepsilon$ and $\mathrm{proj}^*(w.a) = \mathrm{proj}^*(w).\mathrm{proj}(a)$

  1. on input $d \in \mathcal{D}$, if P terminates then P′ terminates
  2. on input $d \in \mathcal{D}$, $\mathrm{proj}^*(\rho) = \mathrm{proj}^*(\rho')$
- a sub-program P′ can be effectively computed (no optimal one)
  compute data dependences and control dependences

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$$\begin{array}{rlllll} \text{run of P on d} & \varrho = (i_0, v_0) & (i_1, v_1) & \cdots & (i_k, v_k) & \cdots & (i_n, v_n) \\ \text{run of P′ on d} & \varrho' = (i'_0, v'_0) & (i'_1, v'_1) & \cdots & (i'_l, v'_l) & \cdots & (i'_m, v'_m) \end{array}$$

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$$\begin{array}{lccccccc} \text{run of P on d} & \varrho = (i_0,v_0) & (i_1,v_1) & \cdots & (i_k,v_k) & \cdots & (i_n,v_n) \\ \text{run of P′ on d} & \varrho' = (i'_0,v'_0) & (i'_1,v'_1) & \cdots & (i'_l,v'_l) & \cdots & (i'_m,v'_m) \end{array}$$

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  - for sequences of pairs: $\text{proj}^*(\varepsilon) = \varepsilon$ and $\text{proj}^*(w.a) = \text{proj}^*(w).\text{proj}(a)$

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Computing a WCET-equivalent Slice

Assume CFG of P is known

Slice criterion C

- each memory transfer instruction is in the criterion C
  `32:ldr r2,[r1,#4]` (32,r1)
- each conditional branch instruction is in C
  `36:beq 34`

What's in the Slice ?

1. initially slice $S = C$ (memory transfers and conditional branching)
2. add to S instructions and variables that define the values of vars in S
   e.g., `28:add r1,r3,#1`
3. add to S instructions and variables that influence the control flow
   e.g., "hidden" loop counters, variables used in comparisons
4. repeat from (2) until fixpoint is reached

Key Result [Weiser 1984]
A slice can be automatically computed.

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Measuring Execution-Time on the ARM920T

```
#define timerToCPUClockRatio 12

main ()
{
  int result;
  unsigned int start;
  unsigned int stop;

  start = timerGetValue(1);
  result = fib(300);
  stop = timerGetValue(1);
  printf("fib(300):␣%d,␣time=%lu\n", result,
                (stop-start)*timerToCPUClockRatio);
  while (1);
}
```

- Embedded hardware timer: 1/12th of processor clock frequency
- measurement error is ± 24 cycles
- a program executing in ≥ 1200 cycles may be accurately measured less than 1% of measurement error

Compiled Program

```
00003214 <fib>:
 0003214: e24dd020  sub sp, sp, #32
 0003218: e58d0004  str r0, [sp, #4]
 000321c: e3a03001  mov r3, #1
 .....
 0003288: e12fff1e  bx lr

0000328c <printbin>:
 000328c: e52de004  bx lr

0000332c <timerGetRegisterAddress>:
 000332c: e24dd008  sub sp, sp, #8
 0003330: e58d0004  str r0, [sp, #4]
 0003334: e58d1000  str r1, [sp]
 0003338: e59d3004  ldr r3, [sp, #4]
 000333c: e3530001  cmp r3, #1
 0003340: 1a000003  bne 0003354 <timerGetRegisterAddress+0x28>
 0003344: e59d3000  ldr r3, [sp]
 0003348: e2833602  add r3, r3, #2097152 ; 0x200000
 000334c: e2833a02  add r3, r3, #8192 ; 0x2000
 0003350: ea000002  b  0003360 <timerGetRegisterAddress+0x34>
 0003354: e59d3000  ldr r3, [sp]
 0003358: e2833602  add r3, r3, #2097152 ; 0x200000
 000335c: e2833a03  add r3, r3, #12288 ; 0x3000
 0003360: e1a00003  mov r0, r3
 0003364: e28dd008  add sp, sp, #8
 0003368: e12fff1e  bx lr

0000336c <timerInit>:
 000336c: e52de004 bx  lr

000033a8 <timerSetPrescaler>:
 00033a8: e52de004 bx  lr
```

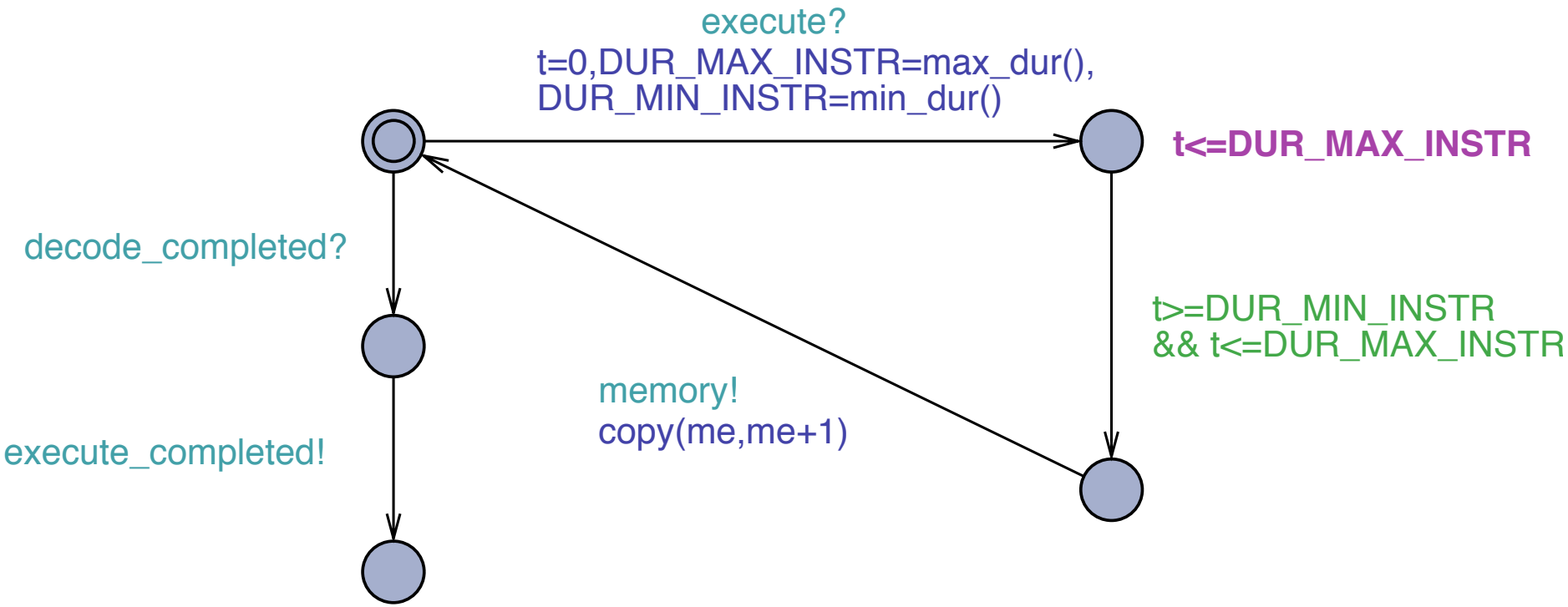
```
000033e4 <timerGetValue>:
 00033e4: e52de004  push {lr}
 00033e8: e24dd014  sub sp, sp, #20
 00033ec: e58d0004  str r0, [sp, #4]
 00033f0: e59d0004  ldr r0, [sp, #4]
 00033f4: e3a01010  mov r1, #16
 00033f8: ebffffcb  bl 000332c <timerGetRegisterAddress>
 00033fc: e1a03000  mov r3, r0
 0003400: e58d300c  str r3, [sp, #12]
 0003404: e59d300c  ldr r3, [sp, #12]
 0003408: e5933000  ldr r3, [r3]
 000340c: e58d3008  str r3, [sp, #8]
 0003410: e59d3008  ldr r3, [sp, #8]
 0003414: e1a00003  mov r0, r3
 0003418: e28dd014  add sp, sp, #20
 000341c: e49df004  pop {pc}

00004ce8 <main>:
 0004ce8: e52de004  push {lr}
 0004cec: e24dd014  sub sp, sp, #20
 0004cf0: e3a00001  mov r0, #1
 0004cf4: e3a01002  mov r1, #2
 0004cf8: ebfff99b  bl 000336c <timerInit>
 0004cfc: e3a00001  mov r0, #1
 0004d00: e3a01000  mov r1, #0
 0004d04: ebfff9a7  bl 00033a8 <timerSetPrescaler>
 0004d08: ebfffe64  mov r0, r0
 ...
 0004d44: ebfff9a6  bl 00033e4 <timerGetValue>
 0004d48: e1a03000  mov r3, r0
 0004d4c: e58d3004  str r3, [sp, #4]
 0004d50: e3a00f4b  mov r0, #300
 0004d54: ebfff92e  bl 0003214 <fib>
 0004d58: e1a03000  mov r3, r0
 0004d5c: e58d3000  str r3, [sp]
 0004d60: e3a00001  mov r0, #1
 0004d64: ebfff99e  bl 00033e4 <timerGetValue>
 0004d68: e1a03000  mov r3, #3
 ...
```

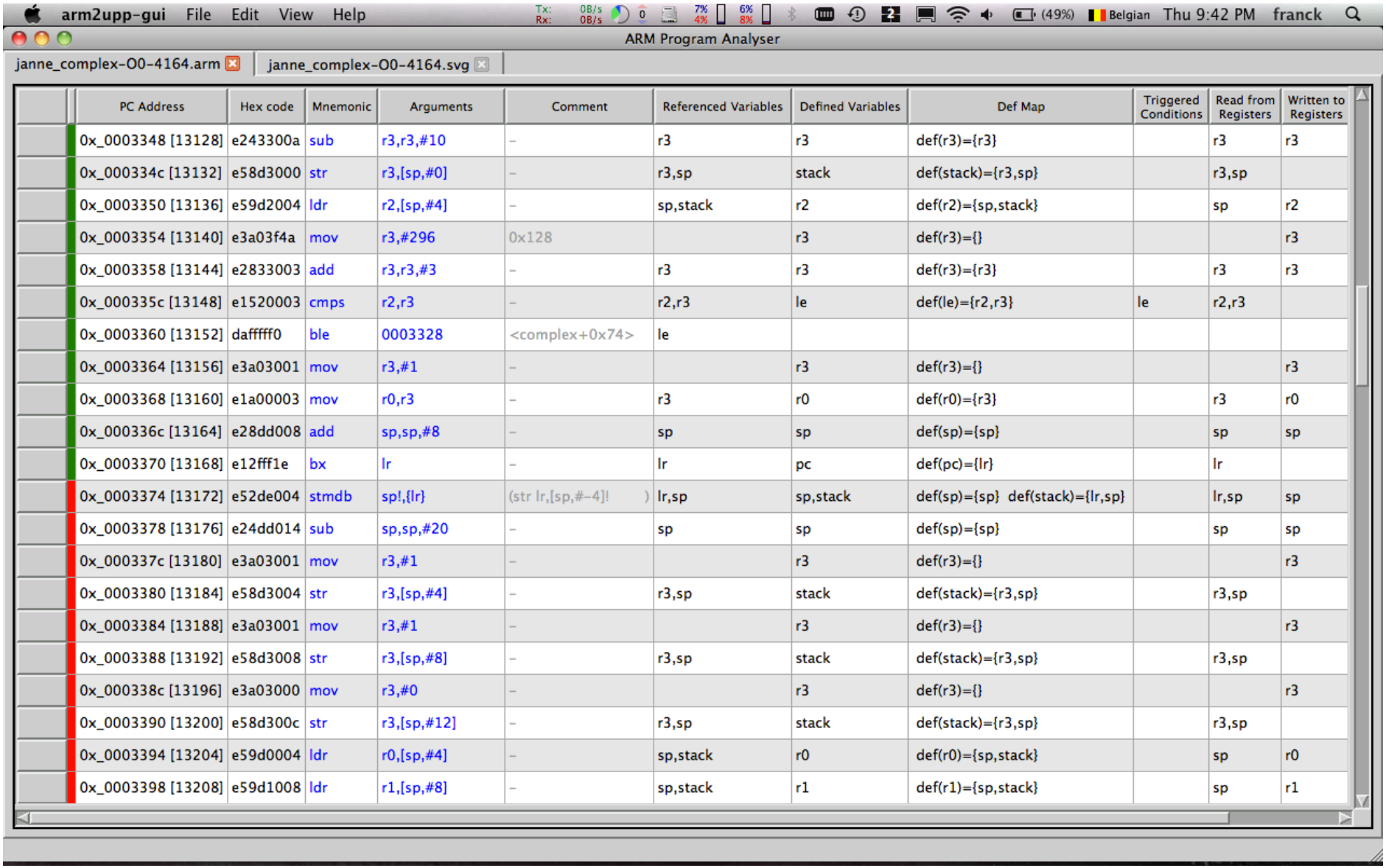
Compiled Program

```
...
0004d44: ebfff9a6  bl 00033e4 <timerGetValue>
0004d48: e1a03000  mov r3, r0
0004d4c: e58d3004  str r3, [sp, #4]
0004d50: e3a00f4b  mov r0, #300
0004d54: ebfff92e  bl 0003214 <fib>
0004d58: e1a03000  mov r3, r0
0004d5c: e58d3000  str r3, [sp]
0004d60: e3a00001  mov r0, #1
0004d64: ebfff99e  bl 00033e4 <timerGetValue>
0004d68: e1a03000  mov r3, #3
...
```

Interval in Execute Stage



Qt GUI



PC Address	Hex code	Mnemonic	Arguments	Comment	Referenced Variables	Defined Variables	Def Map	Triggered Conditions	Read from Registers	Written to Registers
0x_0003348 [13128]	e243300a	sub	r3,r3,#10	-	r3	r3	def(r3)={r3}		r3	r3
0x_000334c [13132]	e58d3000	str	r3,[sp,#0]	-	r3,sp	stack	def(stack)={r3,sp}		r3,sp	
0x_0003350 [13136]	e59d2004	ldr	r2,[sp,#4]	-	sp,stack	r2	def(r2)={sp,stack}		sp	r2
0x_0003354 [13140]	e3a03f4a	mov	r3,#296	0x128		r3	def(r3)={}			r3
0x_0003358 [13144]	e2833003	add	r3,r3,#3	-	r3	r3	def(r3)={r3}		r3	r3
0x_000335c [13148]	e1520003	cmps	r2,r3	-	r2,r3	le	def(le)={r2,r3}	le	r2,r3	
0x_0003360 [13152]	daffffff0	ble	0003328	<complex+0x74>	le					
0x_0003364 [13156]	e3a03001	mov	r3,#1	-		r3	def(r3)={}			r3
0x_0003368 [13160]	e1a00003	mov	r0,r3	-	r3	r0	def(r0)={r3}		r3	r0
0x_000336c [13164]	e28dd008	add	sp,sp,#8	-	sp	sp	def(sp)={sp}		sp	sp
0x_0003370 [13168]	e12fff1e	bx	lr	-	lr	pc	def(pc)={lr}		lr	
0x_0003374 [13172]	e52de004	stmdb	sp!,{lr}	(str lr,[sp,#-4]!)	lr,sp	sp,stack	def(sp)={sp} def(stack)={lr,sp}		lr,sp	sp
0x_0003378 [13176]	e24dd014	sub	sp,sp,#20	-	sp	sp	def(sp)={sp}		sp	sp
0x_000337c [13180]	e3a03001	mov	r3,#1	-		r3	def(r3)={}			r3
0x_0003380 [13184]	e58d3004	str	r3,[sp,#4]	-	r3,sp	stack	def(stack)={r3,sp}		r3,sp	
0x_0003384 [13188]	e3a03001	mov	r3,#1	-		r3	def(r3)={}			r3
0x_0003388 [13192]	e58d3008	str	r3,[sp,#8]	-	r3,sp	stack	def(stack)={r3,sp}		r3,sp	
0x_000338c [13196]	e3a03000	mov	r3,#0	-		r3	def(r3)={}			r3
0x_0003390 [13200]	e58d300c	str	r3,[sp,#12]	-	r3,sp	stack	def(stack)={r3,sp}		r3,sp	
0x_0003394 [13204]	e59d0004	ldr	r0,[sp,#4]	-	sp,stack	r0	def(r0)={sp,stack}		sp	r0
0x_0003398 [13208]	e59d1008	ldr	r1,[sp,#8]	-	sp,stack	r1	def(r1)={sp,stack}		sp	r1

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